XILINX®

XC1700D Family of Serial Configuration PROMs

June 1, 1996 (Version 1.0)

Product Specification

Features

- Extended family of one-time programmable (OTP) bit-serial read-only memories used for storing the configuration bitstreams of Xilinx FPGAs
- On-chip address counter, incremented by each rising edge on the clock input
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- XC17128D or XC17256D supports XC4000 fast configuration mode (12.5 MHz)
- Low-power CMOS EPROM process
- Available in 5 V and 3.3 V versions
- Available in plastic and ceramic packages, and commercial, industrial and military temperature ranges
- Space efficient 8-pin DIP, 8-pin SOIC, 8-pin VOIC, or 20-pin surface-mount packages.
- Programming support by leading programmer manufacturers.

Description

The XC1700 family of serial configuration PROMs (SCPs) provides an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in master serial mode, it generates a configuration clock that drives the SCP. A short access time after the rising clock edge, data appears on the SCP DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SCP. When the FPGA is in slave mode, the SCP and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SCPs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, the XACT development system compiles the FPGA design file into a standard Hex format, which is then transferred to the programmer.
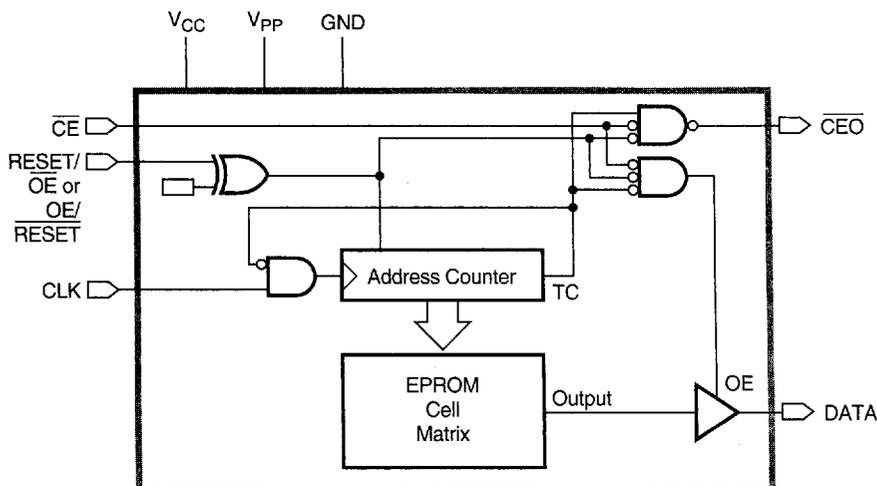
X3185

Figure 1: Simplified Block Diagram (does not show programming circuit)

Pin Description

DATA

Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGA's $\overline{INIT}$ pin.

The polarity of this pin is controlled in the programmer interface by writing data into four high-end byte locations. This input pin is easily inverted using the Xilinx PROM programmer software (XPP). Third-party programmers have different methods to invert this pin.

For RESET/$\overline{OE}$, fill the four polarity bytes with Ones or do nothing.

For $\overline{RESET}$/OE, fill these four bytes with Zeros.

$\overline{CE}$

When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable output, to be connected to the $\overline{CE}$ input of the next SCP in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. *Do not leave VPP floating!*

V_{CC}

Positive supply pin.

GND

Ground pin.

Serial PROM Pinouts

Pin Name	8-Pin	20-Pin
DATA	1	2
CLK	2	4
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	6
$\overline{CE}$	4	8
GND	5	10
$\overline{CEO}$	6	14
V_{PP}	7	17
V_{CC}	8	20

Capacity

Device	Configuration Bits
XC1718D or L	18,144
XC1736D	36,288
XC1765D or L	65,536
XC17128D or L	131,072
XC17256D or L	262,144

plus 32 bits for reset polarity control

Number of Configuration Bits, Including Header for all Xilinx FPGAs and Compatible SCP Type

Device	Configuration Bits	SCP
XC3020/A/L+3120A	14,819	XC1718D
XC3030/A/L+3130A	22,216	XC1736D
XC3042/A/L+3142A	30,824	XC1736D
XC3064/A/L+3164A	46,104	XC1765D
XC3090/A/L+3190A	64,200	XC1765D
XC3195A	94,984	XC17128D
XC4003E	53,976	XC1765D
XC4005E/L	95,000	XC17128D/L
XC4006E	119,832	XC17128D
XC4008E	147,544	XC17256D
XC4010E/L	178,136	XC17256D/L
XC4013E/L	247,960	XC17256D/L
XC4020E	329,304	XC17256D + XC17128D
XC4025E	422,168	XC17256D + XC17256D
XC5202	42,416	XC1765D
XC5204	70,704	XC17128D
XC5206	106,288	XC17128D
XC5210	165,488	XC17256D
XC5215	237,744	XC17256D

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Controlling Serial PROMs

Most connections between the FPGA device and the Serial PROM are simple and self-explanatory.

- The DATA output(s) of the of the Serial PROM(s) drives the DIN input of the lead FPGA device.
- The master FPGA CCLK output drives the CLK input(s) of the Serial PROM(s).
- The CEO output of a Serial PROM drives the CE input of the next Serial PROM in a daisy chain (if any).
- The RESET/OE input of all Serial PROMs is best driven by the INIT output of the XC3000 or XC4000 lead FPGA device. This connection assures that the Serial PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods – such as driving RESET/OE from LDC or system reset – assume that the Serial PROM internal power-on-reset is always in step with the FPGA's internal power-on-reset, which may not be a safe assumption.
- The CE input of the lead (or only) Serial PROM is driven by the DONE/PRGM or DONE output of the lead FPGA device, provided that DONE/PRGM is not permanently grounded. Otherwise, LDC can be used to drive CE, but must then be unconditionally High during user operation. CE can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Logic Cell Array and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The Serial Configuration PROM has been designed for compatibility with the Master Serial Mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial Mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The XC3000 and XC4000 families take care of this automatically with an on-chip default pull-up resistor. With XC2000-family devices, the user must either configure DIN as an active output, or provide a defined level, e.g., by using an external pull-up resistor, if DIN is configured as an input.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a Serial Configuration PROM, the OE pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the OE pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the D/P line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies RESET during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the Serial PROM does not reset its address counter, since it never saw a High level on its OE input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (24) and D/P goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Serial Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded SCPs provide additional memory. After the last bit from the first SCP is read, the next clock signal to the SCP asserts its CEO output Low and disables its DATA line. The second SCP recognizes the Low level on its CE input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded SCPs are reset if the FPGA RESET pin goes Low, assuming the SCP reset polarity option has been inverted.

To reprogram the FPGA with another program, the D/P line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.
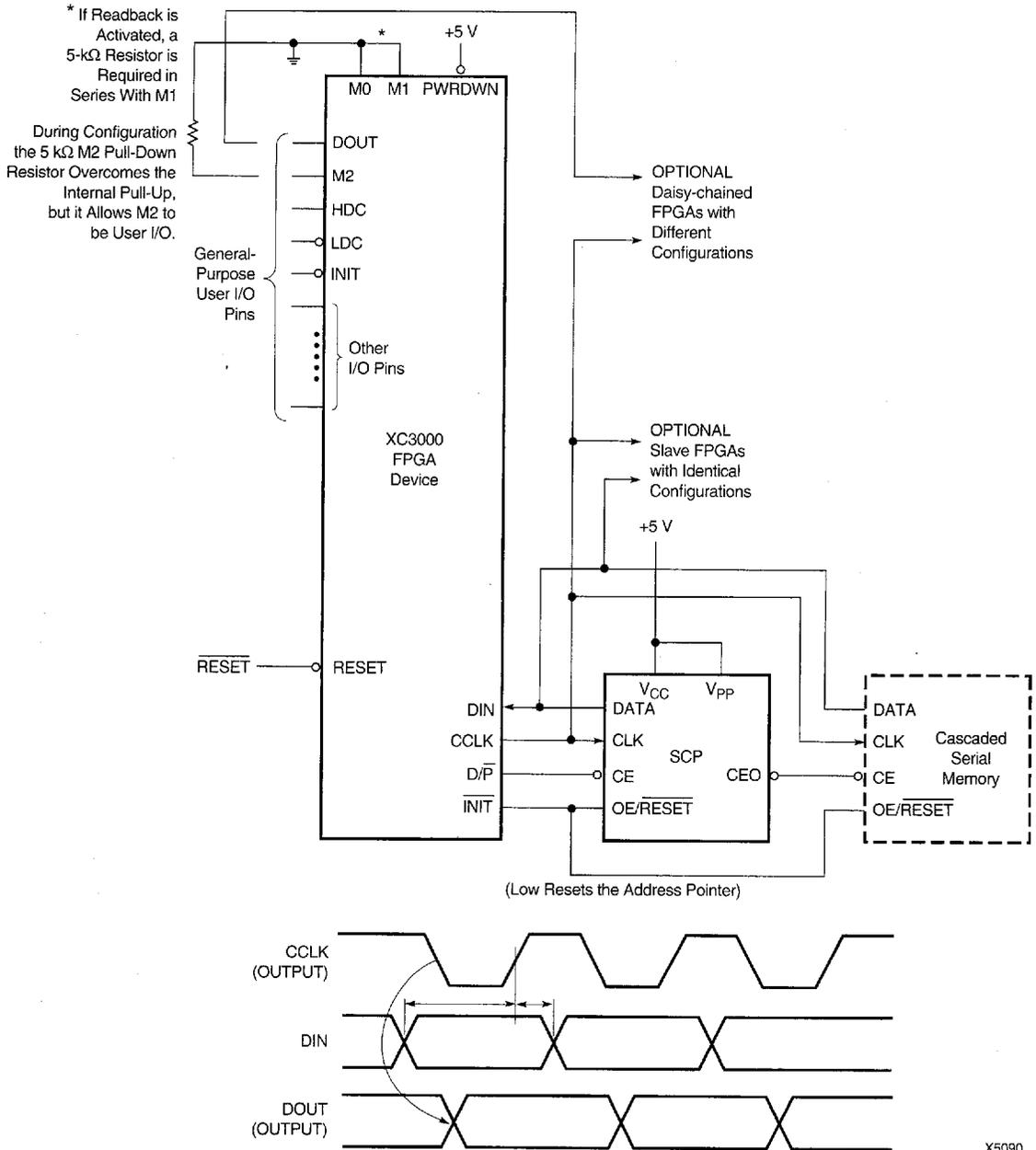
Figure 2: Master Serial Mode. The one-time-programmable Serial Configuration PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGA. An early D/P̄ inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

(A technique for further reducing the standby current of a Serial Configuration PROM is described in the XCELL journal, Issue 11, page 13.)

Programming the XC1700 Family Serial PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and voltages are used. Different product types use different algorithms and voltages, and the wrong choice can permanently damage the device.

Table 1: Truth Table for XC1700 Control Inputs

Control Inputs		Internal Address	Outputs		
RESET	CE		DATA	CEO	I_{cc}
Inactive	Low	if address $\leq$ TC: increment	active	High	active
		if address > TC: don't change	3-state	Low	reduced
Active	Low	Held reset	3-state	High	active
Inactive	High	Not changing	3-state	High	standby
Active	High	Held reset	3-state	High	standby

Notes: 1. The XC1700 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC+1 = address 0.

Table 2: Data I/O Programmer Locations for Programming RESET Polarity

Device	Hex Address
XC1718D or L	8DC through 8DF
XC1736D	11B8 through 11BB
XC1765D or L	2000 through 2003
XC17128D or L	4000 through 4003
XC17256D or L	8000 through 8003

IMPORTANT: Always be sure to use the proper programming algorithm. "D" series PROMs will not program properly using "A" -series algorithms. Always tie the V_{PP} pin to V_{CC} in your application. Never leave V_{PP} floating.

XC1718D, XC1736D, XC1765D, XC17128D and XC17256D

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +125	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND 0°C to +70°C junction	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to +85°C junction	4.50	5.50	V
	Military	Supply voltage relative to GND -55°C to +125°C case	4.50	5.50	V

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10.0	mA
I_{CCS}	Supply current, standby mode, XC17128D, XC17256D			50.0	µA
	Supply current, standby mode, XC1718D, XC1736D, XC1765D			1.5	mA
I_L	Input or output leakage current		-10.0	10.0	µA

Note: During normal read operation V_{PP} **must** be connected to V_{CC}

XC1718L, XC1765L, XC17128L and XC17256L

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +6.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND 0°C to +70°C junction	3.0	3.6	V

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		0.4	V
I_{CCA}	Supply current, active mode		5.0	mA
I_{CCS}	Supply current, standby mode, XC1718L, XC1765L		1.5	mA
	Supply current, standby mode, XC17128L, XC17265L		50.0	µA
I_L	Input or output leakage current	-10.0	10.0	µA

Note: During normal read operation V_{PP} *must* be connected to V_{CC}
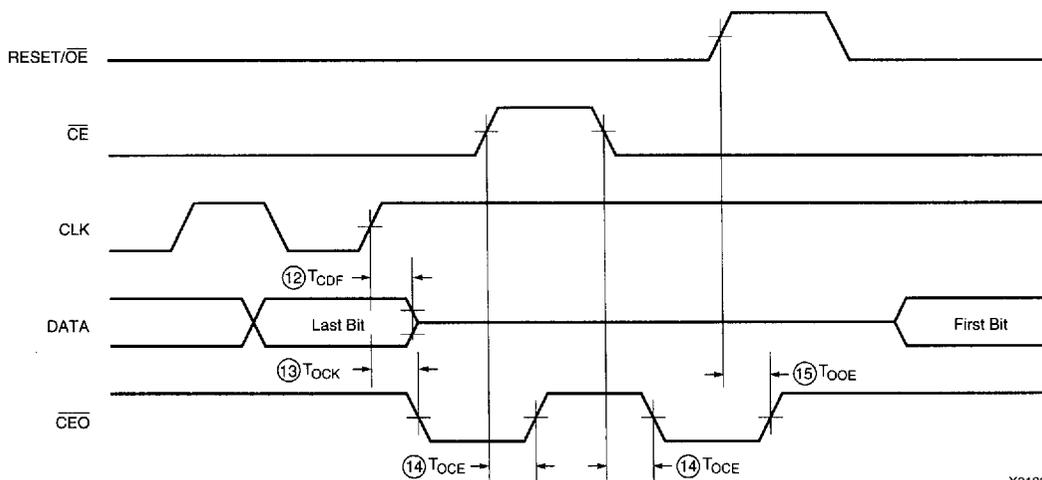
AC Characteristics Over Operating Condition
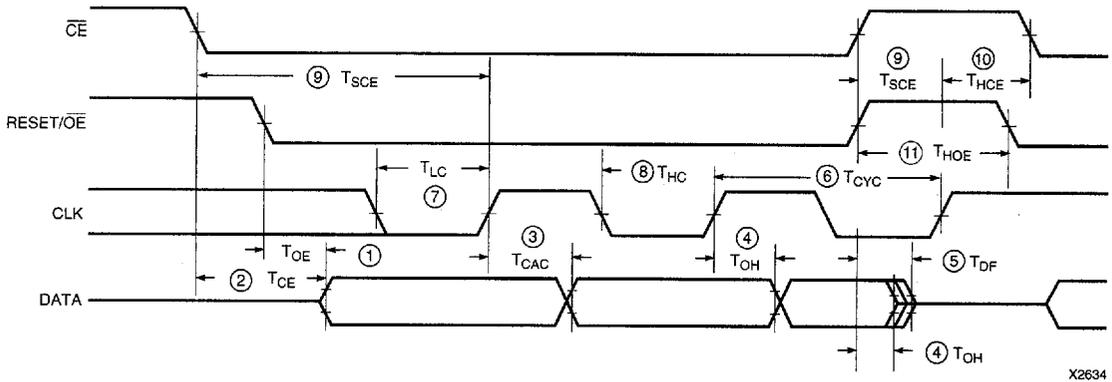
X2634

	Symbol	Description	XC1718D XC1736D XC1765D		XC1718L XC1765L		XC17128D XC17256D		XC17128L XC17256L		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
1	T_{OE}	OE to Data Delay		45		45		25		30	ns
2	T_{CE}	CE to Data Delay		60		60		45		60	ns
3	T_{CAC}	CLK to Data Delay		150		200		50		60	ns
4	T_{OH}	Data Hold From CE, OE, or CLK	0		0		0		0		ns
5	T_{DF}	CE or OE to Data Float Delay[2]		50		50		50		50	ns
6	T_{CYC}	Clock Periods	200		400		80		100		ns
7	T_{LC}	CLK Low Time[3]	100		100		20		25		ns
8	THC	CLK High Time[3]	100		100		20		25		ns
9	TSCE	CE Setup Time to CLK (to guarantee proper counting)	25		40		20		25		ns
10	T_{HCE}	CE Hold Time to CLK (to guarantee proper counting)	0		0		0		0		ns
11	T_{HOE}	OE Hold Time (guarantees counters are reset)	100		100		20		25		ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with minimum tester ac load and maximum dc load.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

AC Characteristics Over Operating Condition (continued)

X3183

Symbol		Description	XC1718D XC1736D XC1765D		XC1718L XC1765L		XC17128D XC17256D		XC17128L XC17256L		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
12	T_{CDF}	CLK to Data Float Delay[2]		50		50		50		50	ns
13	T_{OCK}	CLK to CEO Delay		65		65		30		30	ns
14	T_{OCE}	CE to CEO Delay		45		45		35		35	ns
15	T_{OOE}	RESET/OE to CEO Delay		40		40		30		30	ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with minimum tester ac load and maximum dc load.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with $V_{IL} = 0.0$ V and $V_{IH} = 3.0$ V.

Ordering Information

XC1736D - PC20 C

Device Number
XC1718D
XC1718L
XC1736D
XC1765D
XC1765L
XC17128D
XC17128L
XC17256D
XC17256L

Package Type
PD8 = 8-Pin Plastic DIP
DD8 = 8-Pin CerDIP
SO8 = 8-Pin Plastic Small-Outline Package
VO8 = 8-Pin Plastic Small-Outline Thin Package
PC20 = 20-Pin Plastic Leaded Chip Carrier

Operating Range/Processing
C = Commercial (0° to +70°C)
I = Industrial (–40° to +85°C)
M = Military (–55° to +125°C)
B = Military (–55° to +125°C)
    MIL-STD-883 Level B compliant

Valid Ordering Combinations

XC17128DPD8C	XC1718DPD8C	XC17256DPD8C	XC1736DPD8C	XC1765DPD8C
XC17128DVO8C	XC1718DSO8C	XC17256DVO8C	XC1736DSO8C	XC1765DSO8C
XC17128DPC20C	XC1718DVO8C	XC17256DPC20C	XC1736DVO8C	XC1765DVO8C
XC17128DPD8I	XC1718DPC20C	XC17256DPD8I	XC1736DPC20C	XC1765DPC20C
XC17128DVO8I	XC1718DPD8I	XC17256DVO8I	XC1736DPD8I	XC1765DPD8I
XC17128DPC20I	XC1718DSO8I	XC17256DPC20I	XC1736DSO8I	XC1765DSO8I
XC17128DDD8M	XC1718DVO8I	XC17256DDD8M	XC1736DVO8I	XC1765DVO8I
	XC1718DPC20I	XC17256DDD8B	XC1736DPC20I	XC1765DPC20I
			XC1736DDD8M	XC1765DDD8M
				XC1765DDD8B
XC17128LPD8C	XC1718LPD8C	XC17256LPD8C		XC1765LPD8C
XC17128LVO8C	XC1718LSO8C	XC17256LVO8C		XC1765LSO8C
XC17128LPC20C	XC1718LVO8C	XC17256LPC20C		XC1765LVO8C
XC17128LPD8I	XC1718LPC20C	XC17256LPD8I		XC1765LPC20C
XC17128LVO8I	XC1718LPD8I	XC17256LVO8I		XC1765LPD8I
XC17128LPC20I	XC1718LSO8I	XC17256LPC20I		XC1765LSO8I
	XC1718LVO8I			XC1765LVO8I
	XC1718LPC20I			XC1765LPC20I

Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.

1736D   P   C

Device Number
XC1718D
XC1718L
XC1736D
XC1765D
XC1765L
XC17128D
XC17128L
XC17256D
XC17256L

Package Type
P = 8-Pin Plastic DIP
D = 8-Pin CerDIP
S = 8-Pin Plastic Small-Outline Package
V = 8-Pin Plastic Small-Outline Thin Package
J = 20-Pin Plastic Leaded Chip Carrier

Operating Range/Processing
C = Commercial (0° to +70°C)
I = Industrial (–40° to +85°C)
M = Military (–55° to +125°C)
B = Military (–55° to +125°C)
    MIL-STD-883 Level B compliant

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