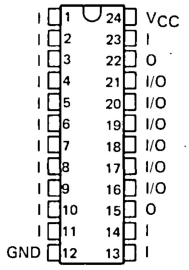
PAL20L8A, PAL20R4A, PAL20R6A, PAL20R8A
STANDARD HIGH SPEED PAL® CIRCUITS

D2706, DECEMBER 1982—REVISED JANUARY 1985

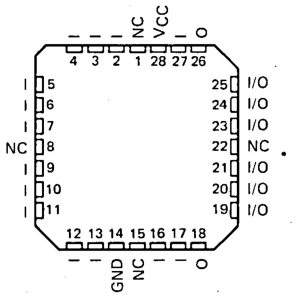
- Standard High Speed (25 ns) PAL Family
- Choice of Operating Speeds
  HIGH SPEED, A devices . . . 30 MHz
  HALF POWER, A-2 devices . . . 18 MHz
- Choice of Input/Output Configuration
- Preload Capability on Output Registers
- DIP Options Include Both 300-mil Plastic and 600-mil Ceramic

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8A	14	2	0	6
'PAL20R4A	12	0	4 (3-state buffers)	4
'PAL20R6A	12	0	6 (3-state buffers)	2
'PAL20R8A	12	0	8 (3-state buffers)	0

PAL20L8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



DIP pin assignments in operating mode (voltages at pins 1 and 13 less then V_{IHH}). PLCC pin assignments in operating mode (voltages at pins 2 and 16 less then V_{IHH}).

description

These programmable array logic devices feature high speed and a choice of either standard or half-power speeds. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

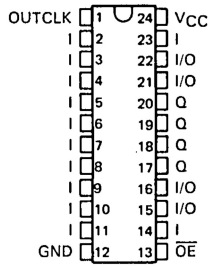
In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The PAL20' series is characterized for operation over the full military temperature range of −55°C to 125°C. The commercial range is characterized from 0°C to 70°C.

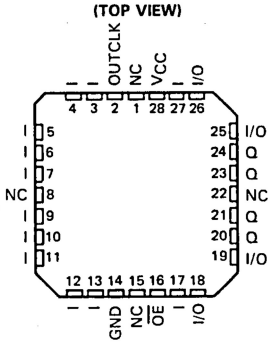
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

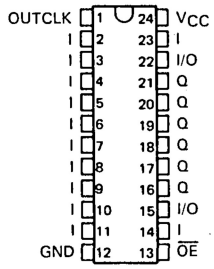
PAL20R4'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20R4'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



PAL20R6'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20R6'
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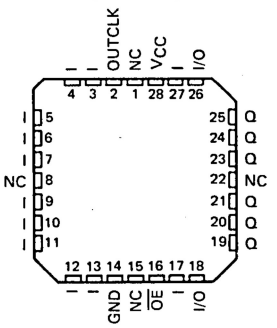
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



PAL20R8'
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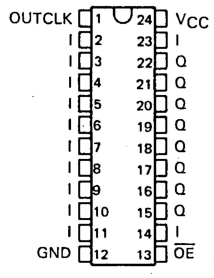
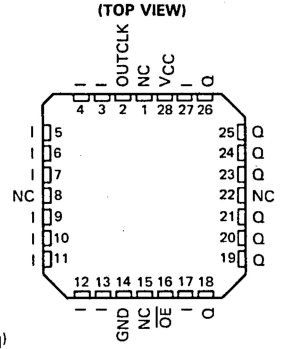
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20R8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



DIP pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})
PLCC pin assignments in operating mode (voltages at pins 2 and 16 less than V_{IHH})

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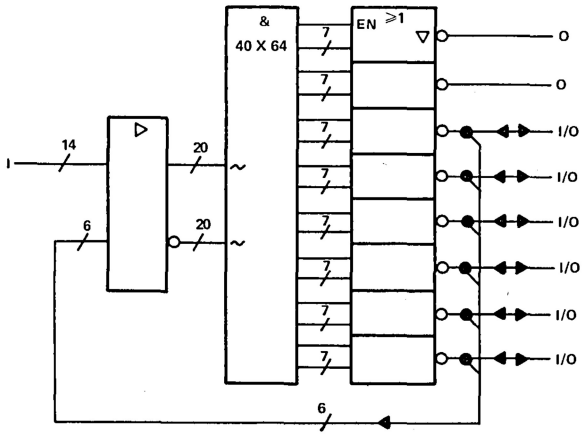
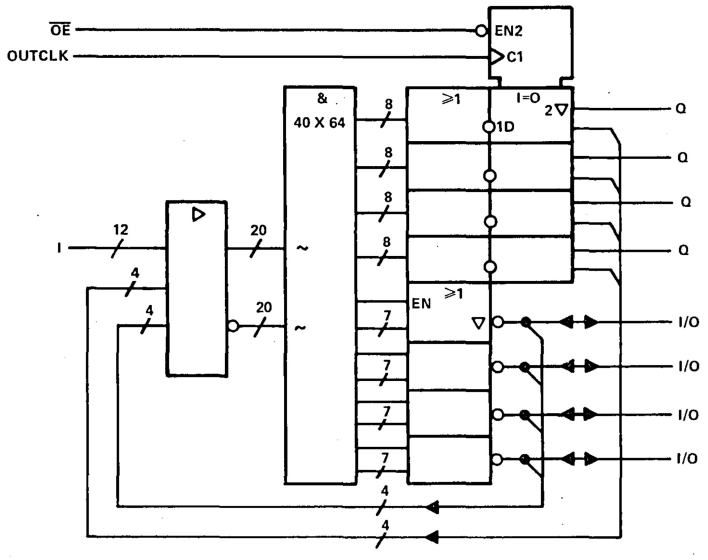
functional block diagrams (positive logic)

PAL20L8A
PAL20L8A-2

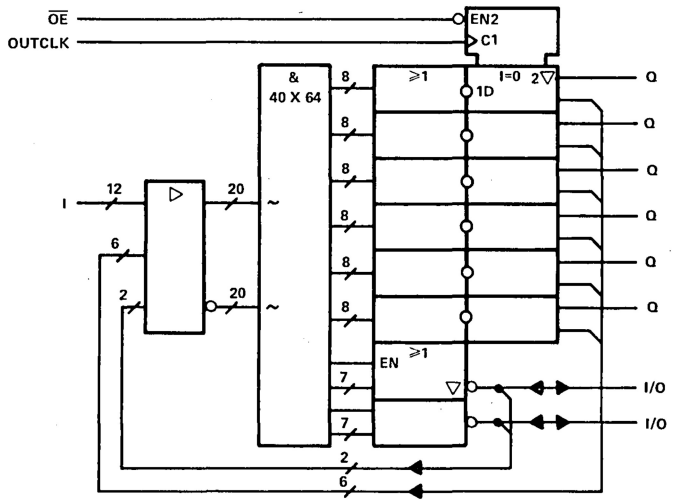


PAL20R4A
PAL20R4A-2

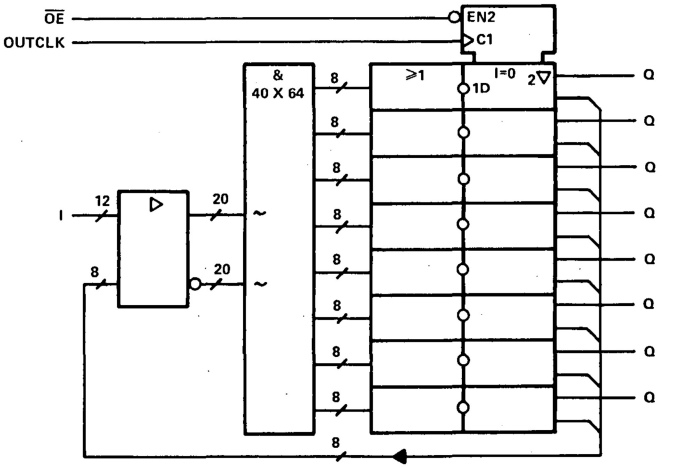


functional block diagrams (positive logic)

PAL20R6A
PAL20R6A-2



PAL20R8A
PAL20R8A-2



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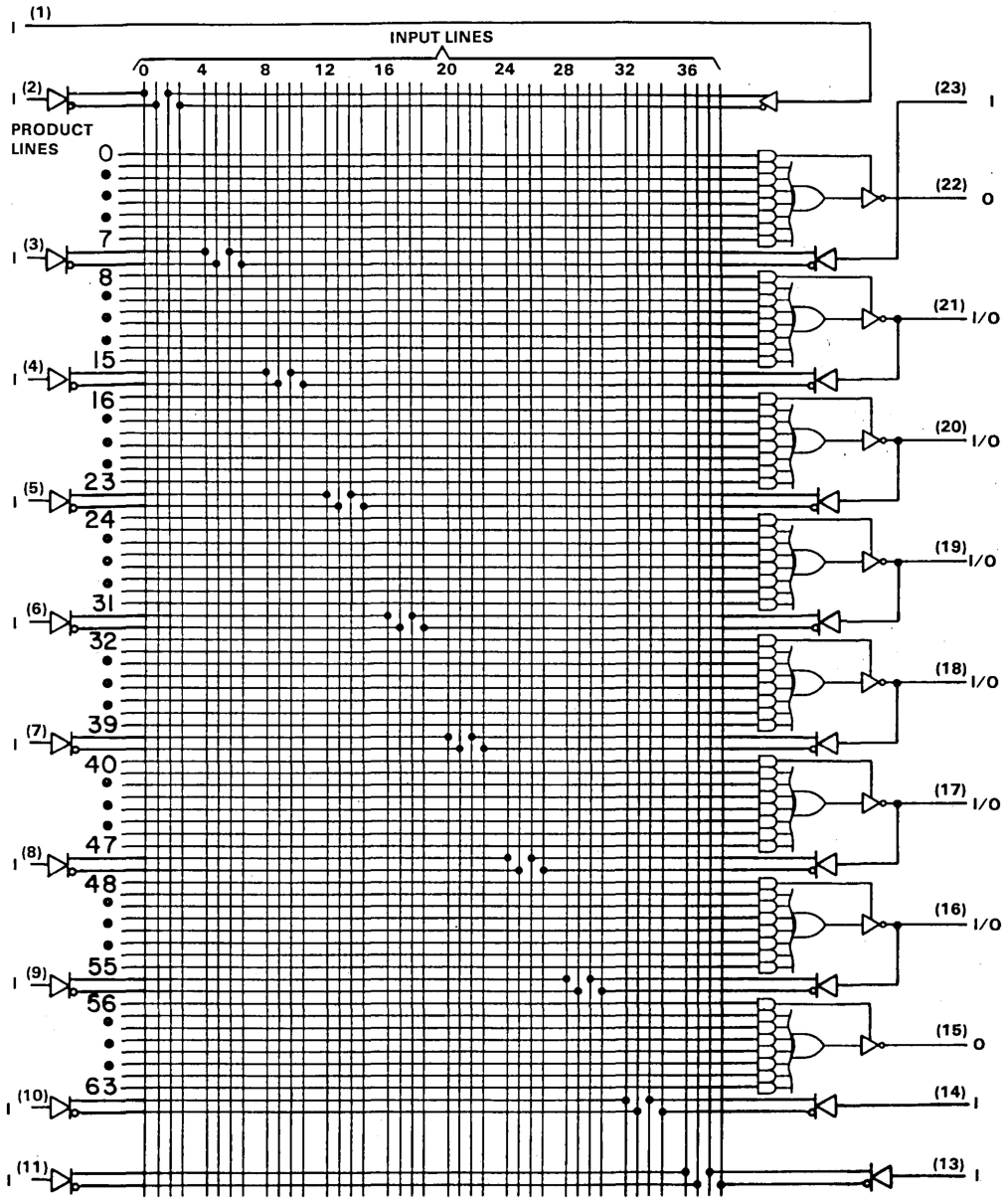
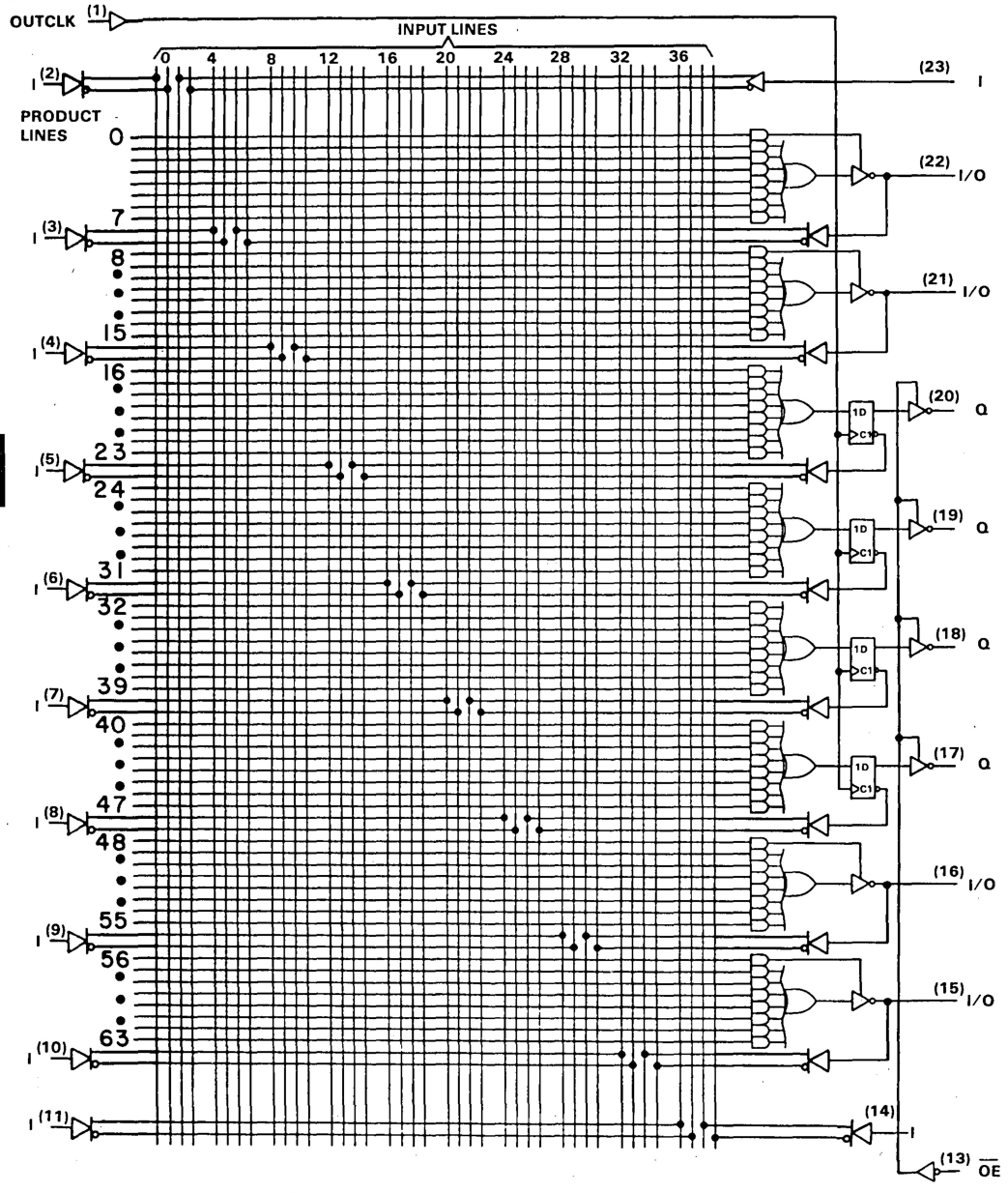

(1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
(2)
PRODUCT LINES
0
7
(3)
8
15
(4)
16
23
(5)
24
31
(6)
32
39
(7)
40
47
(8)
48
55
(9)
56
63
(10)
(11)
(23) I
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) I
(13) I



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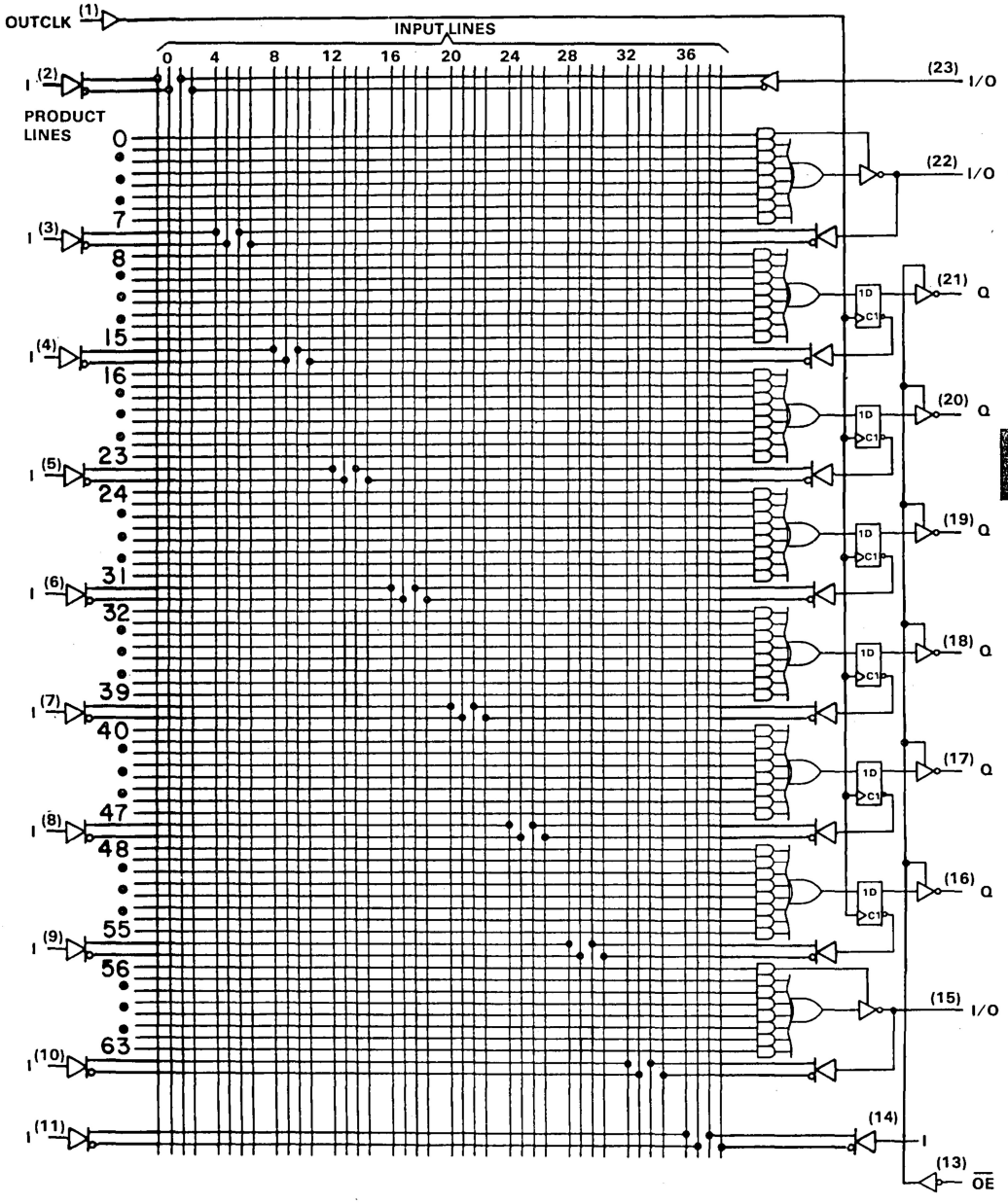
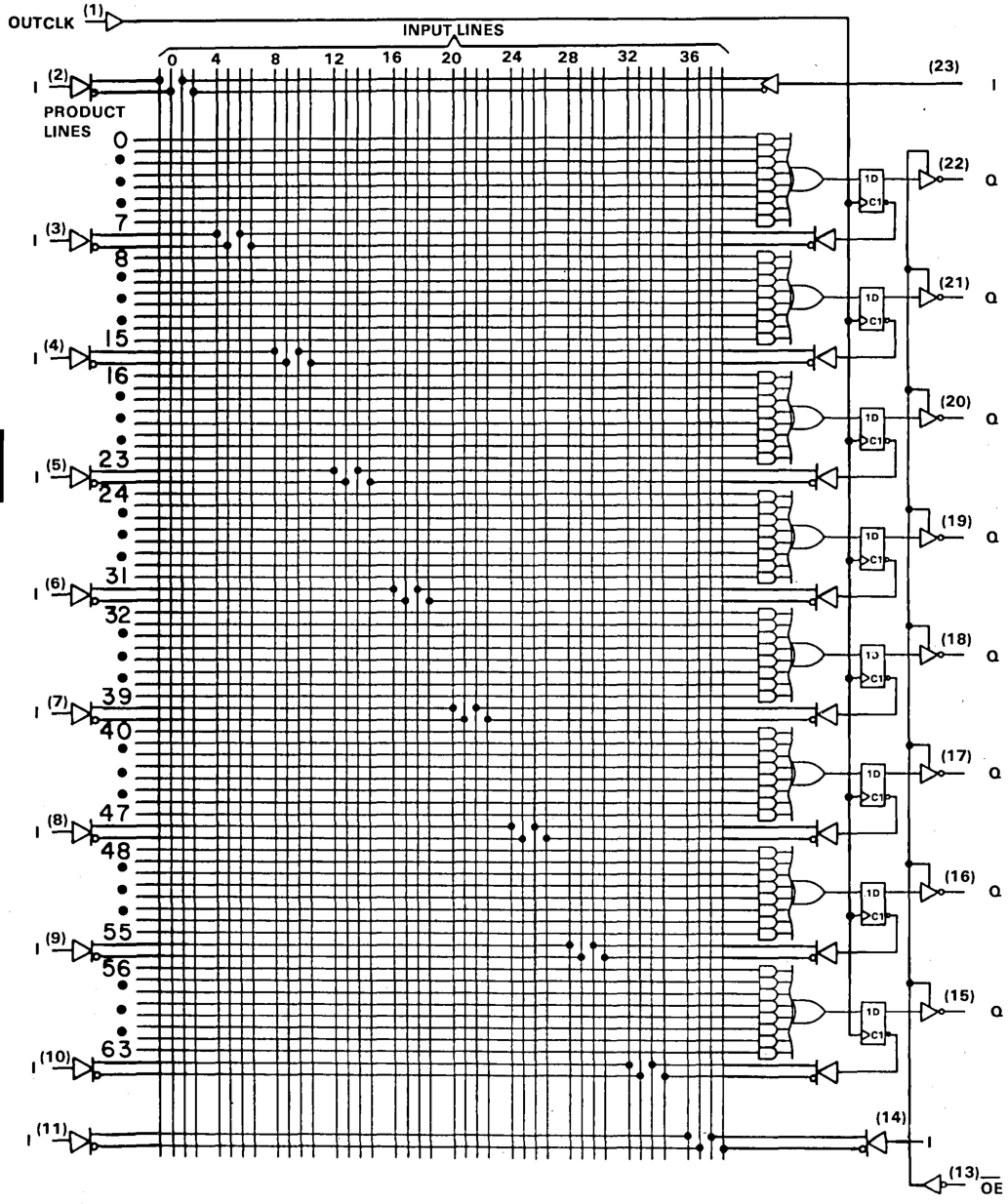

OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
(2)
PRODUCT LINES
0
7
(3)
8
15
(4)
16
23
(5)
24
31
(6)
32
39
(7)
40
47
(8)
48
55
(9)
56
63
(10)
(11)
(23) I/O
(22) I/O
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
(14) I
(13) OE
1D
C1



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER		M SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO		20	50	mA
		PGM ENABLE, L/R		10	25	
		PI, PA		1.5	5	
		V_{CC}		250	400	
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY↑		100			μs
t_{d2}	Delay time from PGM VERIFY↑ to valid output		200			ns
	Input voltage at pins 1 and 11 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
t_{w3}	Pulse duration to open verify-protect (security) fuse		20		50	μs
	V_{CC} value during security fuse programming			0	0.4	V

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		20	0		30	MHz
t_w	Pulse duration, clock	High	20			15			ns
		Low	20			15			ns
t_{su}	Setup time, input or feedback before OUTCLK↑		30			25			ns
t_h	Hold time, input or feedback after OUTCLK↑		0			0			ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = MAX, V_{IH} = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	O, Q outputs	V_{CC} = MAX, V_{IH} = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I	$\overline{OE}$ input	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
	All others				0.1			0.1	
I_{IH}	$\overline{OE}$ input	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
	All others				20			20	
I_{IL}	$\overline{OE}$ input	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	All others				−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs open, $\overline{OE}$ at V_{IH}		150	210		150	210	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				20			30			MHz
t_{pd}	I, I/O	O, I/O			15	30		15	25	ns
t_{pd}	OUTCLK↑	Q	R_L = 500 Ω,		10	20		10	15	ns
t_{en}	$\overline{OE}$	Q	C_L = 50 pF		10	25		10	20	ns
t_{dis}	$\overline{OE}$↑	Q	See Note 2		11	25		11	20	ns
t_{en}	I, I/O	O, I/O			14	30		14	25	ns
t_{dis}	I, I/O	O, I/O			12	30		12	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		18	0		18	MHz
t_w	Pulse duration, clock	High							ns
		Low							ns
t_{su}	Setup time, input or feedback before OUTCLK↑								ns
t_h	Hold time, input or feedback after OUTCLK↑								ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = MAX, V_{IH} = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	O, Q outputs	V_{CC} = MAX, V_{IH} = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
	All others				0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
	All others				20			20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	All others				−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs open, $\overline{OE}$ at V_{IH}		75	100		75	100	mA

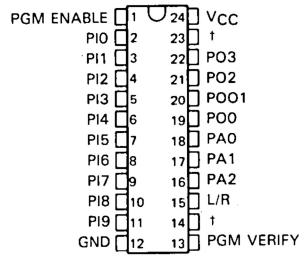
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

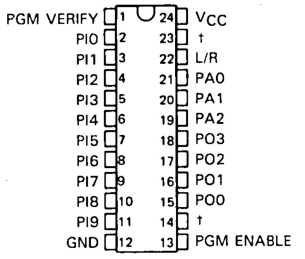
PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF, See Note 2	18			18			MHz
t_{pd}	I, I/O	O, I/O			25			25		ns
t_{pd}	OUTCLK↑	Q			20			20		ns
t_{en}	$\overline{OE}$	Q			15			15		ns
t_{dis}	$\overline{OE}$↑	Q			12			12		ns
t_{en}	I, I/O	O, I/O			25			25		ns
t_{dis}	I, I/O	O, I/O			20			20		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



†Pins 14 and 23 have no programming function. Make no connection.
Pin assignments in programming mode (PGM ENABLE at V_{IHH})

TABLE 1. INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2. PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

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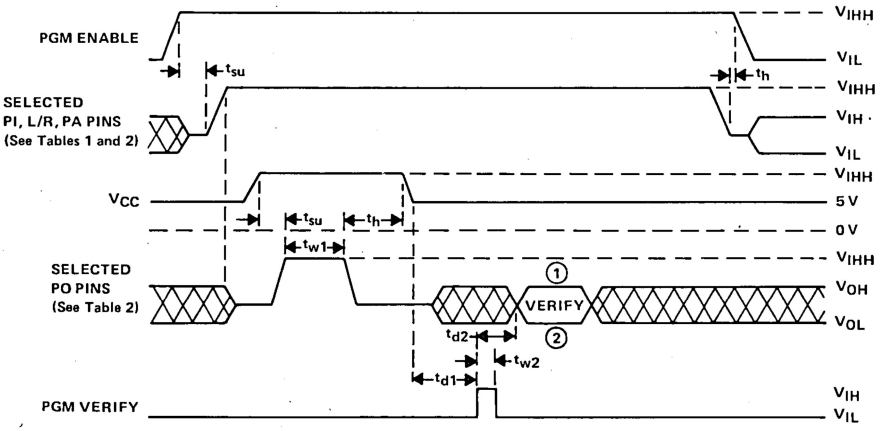
programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 Raise PGM ENABLE to V_{IHH}.
Step 2 Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 Begin selection of the output line with appropriate conditions on PA pins.
Step 4 Raise V_{CC} to V_{IHH}.
Step 5 Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6 Return V_{CC} to 5 volts and pulse PGM Verify. The PO pin selected in Step 5 will be less than V_{OL} if the fuse is open.

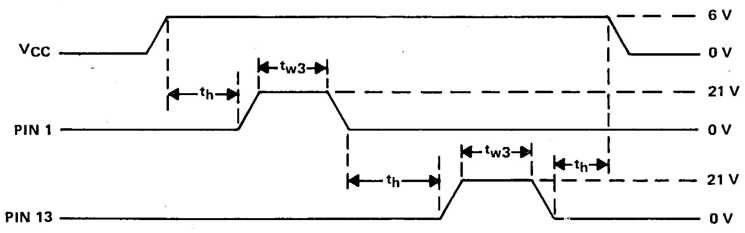
Steps 1 through 6 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than four times. Verification is possible only with the verify-protect fuse intact.

programming waveforms



(1) A high level during the verify interval indicates that programming has not been successful.
(2) A low level during the verify interval indicates that programming has been successful.

security fuse programming



PRELOAD PROCEDURES

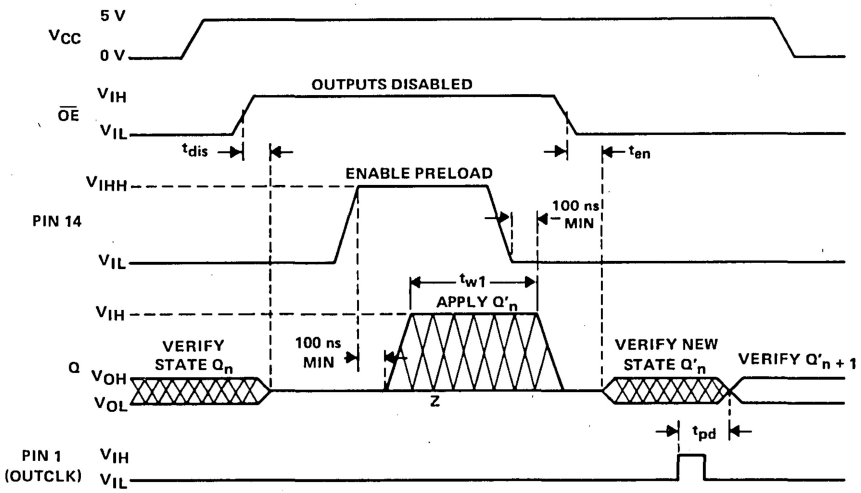


FIGURE 1. PRELOAD WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH} for 10 to 50 microseconds.
Step 3	Apply V_{IL} for a low and V_{IH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

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