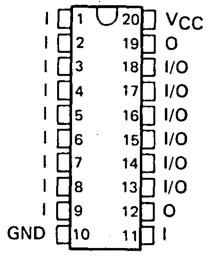
FEBRUARY 1984—REVISED JANUARY 1985

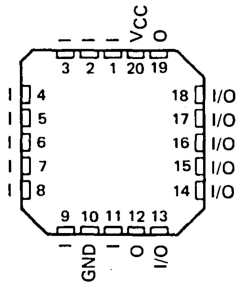
- **Standard High-Speed (25 ns) PAL Family**
- **Choice of Operating Speeds**
  HIGH SPEED, A Devices . . . 35 MHz
  HALF POWER, A-2 Devices . . . 18 MHz
- **Choice of Input/Output Configuration**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

PAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode (pins 1 and 11 less positive than V_{IHH})

description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL16' C series is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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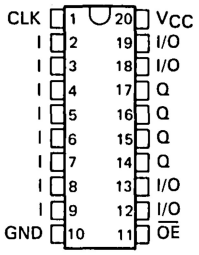
PAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16R4'
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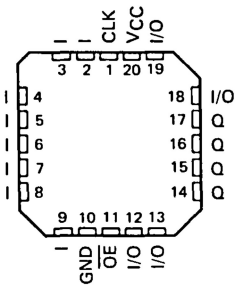
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



PAL16R6'
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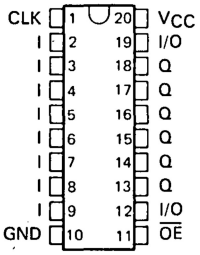
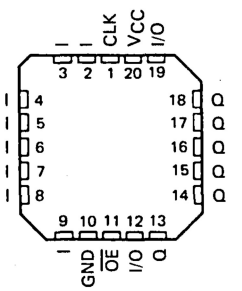
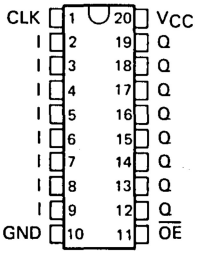
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



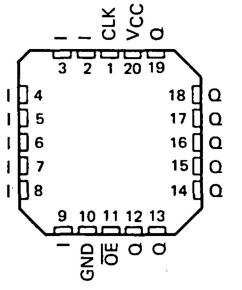
PAL16R6'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



PAL16R8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16R8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode (pins 1 and 11 less positive than V_{IHH})

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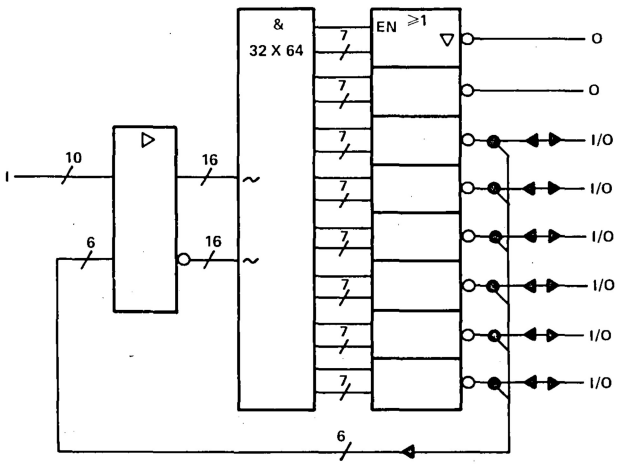
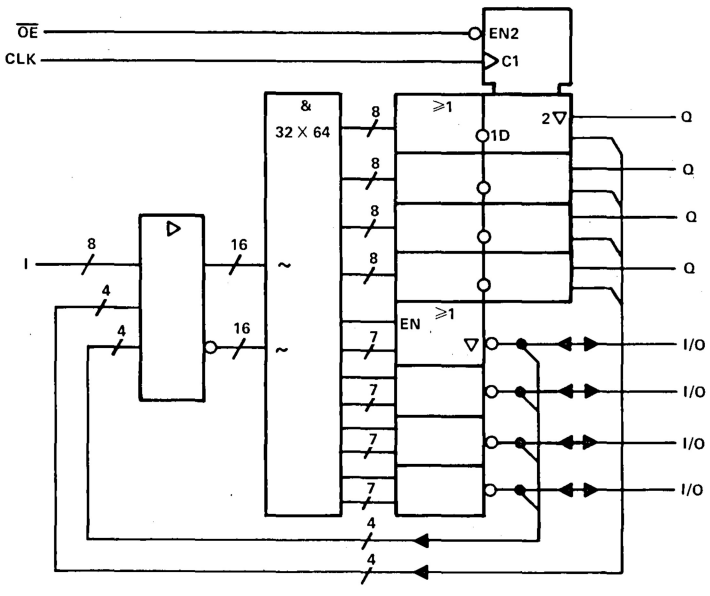
functional block diagrams (positive logic)

'PAL16L8A
'PAL16L8A-2



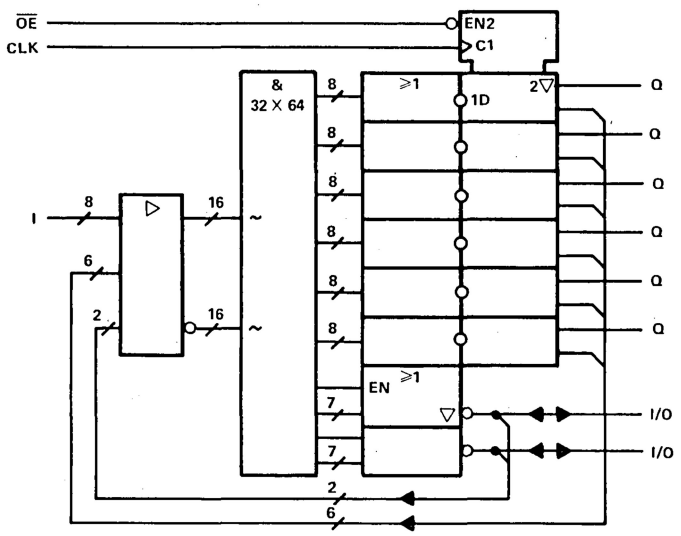
'PAL16R4A
'PAL16R4A-2



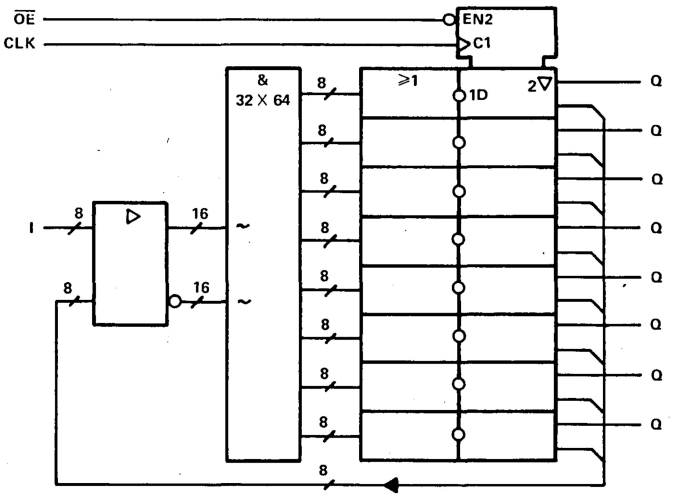
~ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6A
'PAL16R6A-2



'PAL16R8A
'PAL16R8A-2



~ denotes fused inputs

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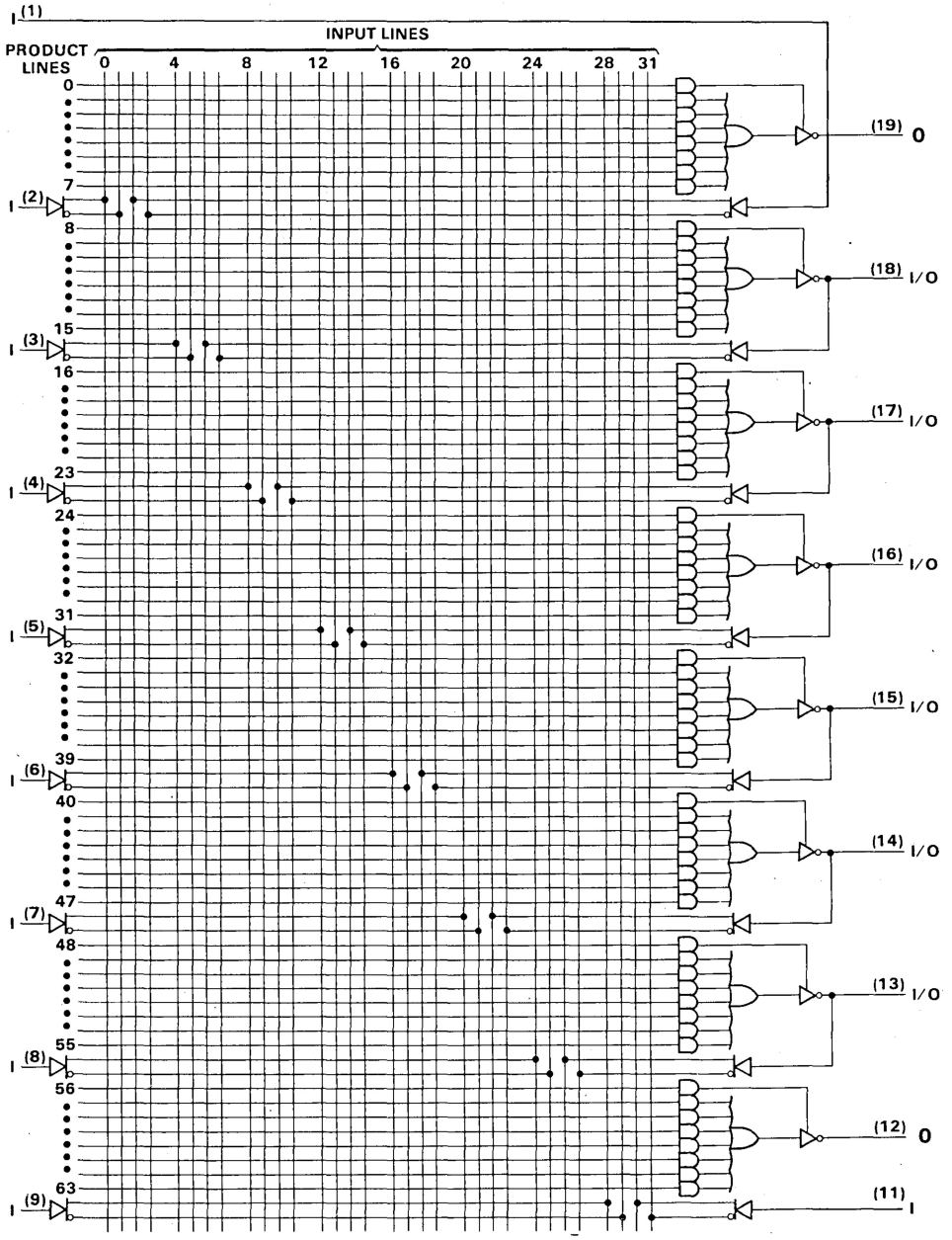
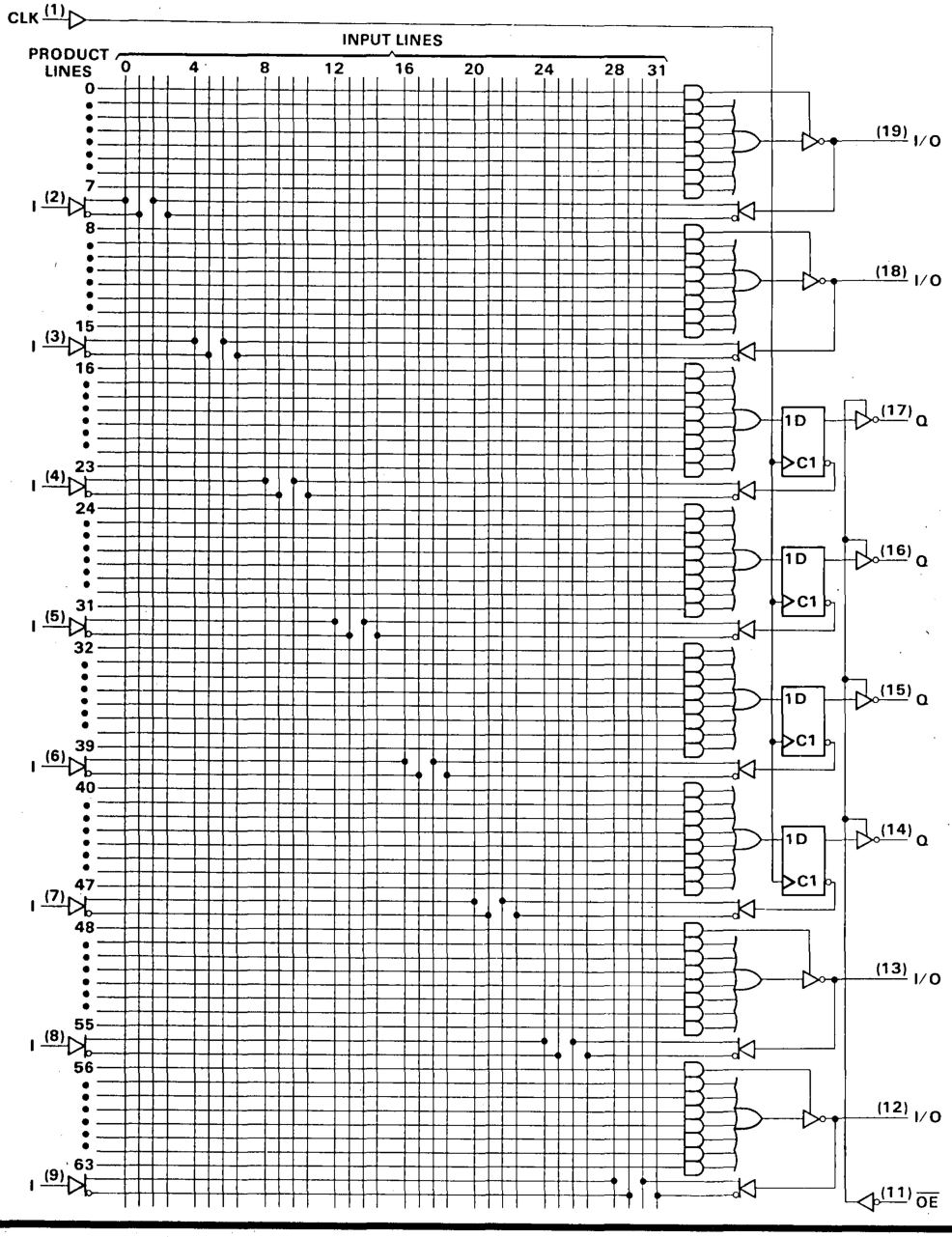
logic diagram



logic diagram



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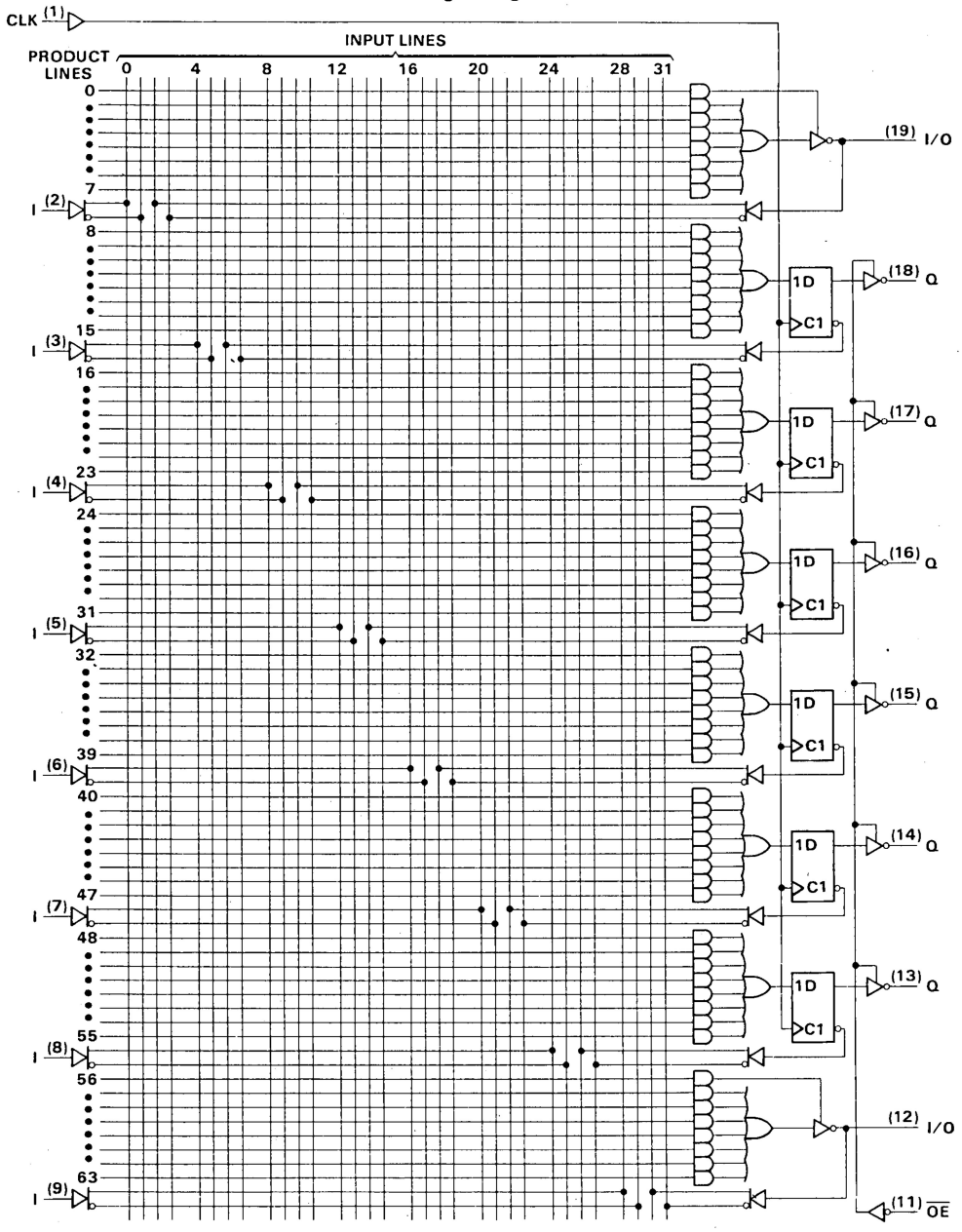
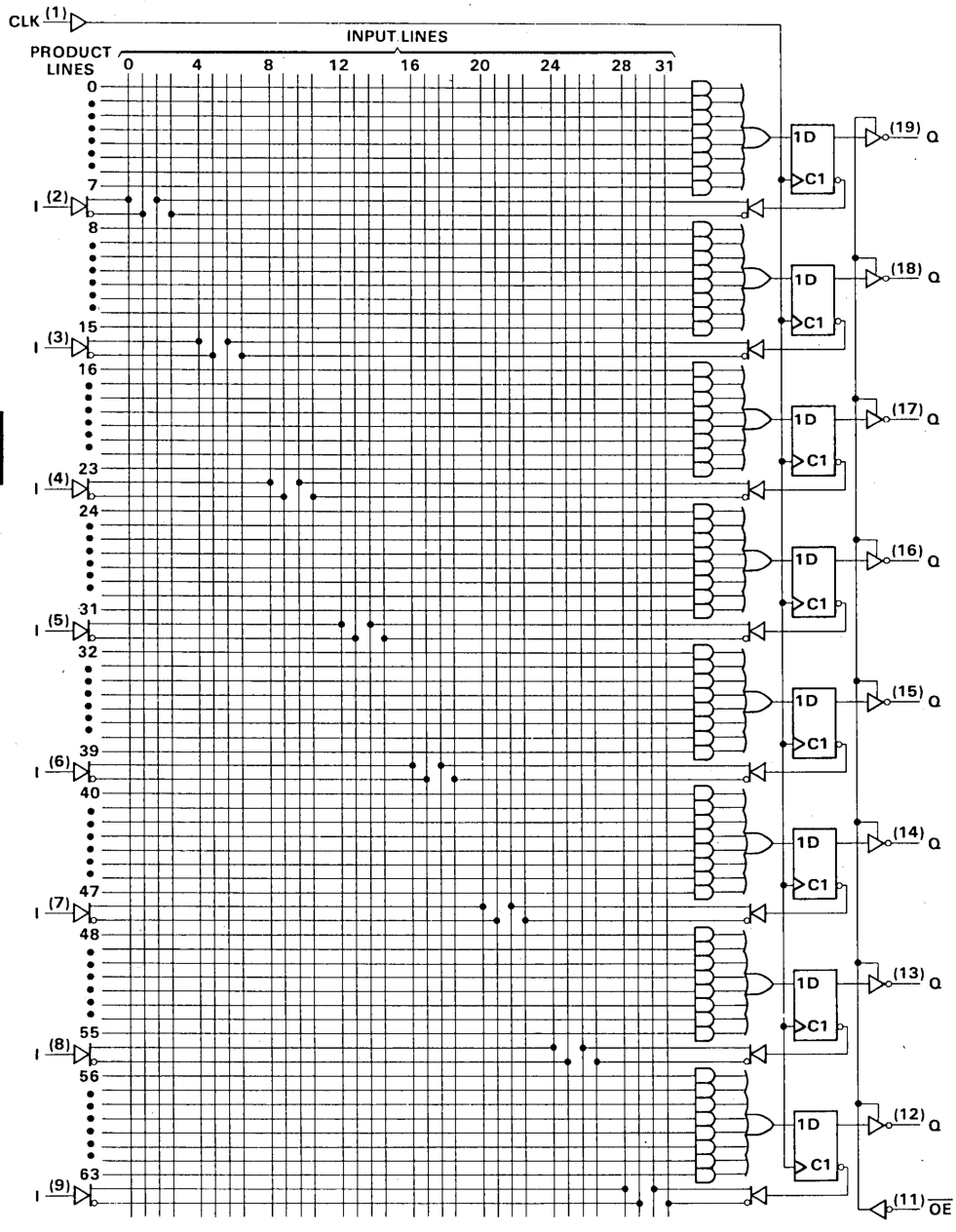
logic diagram



logic diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{OE}$ input	2.4		5.5	2		5.5	V
		All others	2		5.5	2		5.5	
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO		20	50	mA
		PGM ENABLE, L/R		10	25	
		PI, PA		1.5	5	
		V_{CC}		250	400	
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY↑		100			μs
t_{d2}	Delay time from PGM VERIFY ↑ to valid output		200			ns
	Input voltage at pins 1 and 11 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
t_{w3}	Pulse duration to open verify-protect (security) fuse		20		50	μs
	V_{CC} value during security fuse programming			0	0.4	V

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		25	0		35	MHz
t_w	Pulse duration, see Note 2	Clock high	15			12			ns
		Clock low	20			16			
t_{su}	Setup time, input or feedback before CLK↑		25			20			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V				20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V				−20			−20	μA
	I/O ports					−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V				0.2			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				25			20	μA
I_{IL}		V_{CC} = MAX, V_I = 0.4 V	$\overline{OE}$ INPUT			−0.25			−0.4	mA
			All others			−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs Open			140	185		140	180	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF, See Note 3	25	45		35	45		MHz
t_{pd}	I, I/O,	O, I/O			15	30		15	25	ns
t_{pd}	CLK↑	Q			10	20		10	15	ns
t_{en}	$\overline{OE}$↓	Q			15	25		15	22	ns
t_{dis}	$\overline{OE}$↑	Q			10	25		10	15	ns
t_{en}	I, I/O	O, I/O			14	30		14	25	ns
t_{dis}	I, I/O	O, I/O			13	30		13	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		16	0		18	MHz
t_w	Pulse duration, see Note 2	Clock high	28			25			ns
		Clock low	28			25			
t_{su}	Setup time, input or feedback before CLK↑		35			28			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†			M SUFFIX			C SUFFIX			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V				20			20	μA
	I/O ports						100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V				−20			−20	μA
	I/O ports						−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V				0.2			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				25			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V	$\overline{OE}$ INPUT			−0.2			−0.2	mA
				All others			−0.1			−0.1	
I_O§		V_{CC} = MAX,	V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V	Outputs Open			75	95		70	90	mA

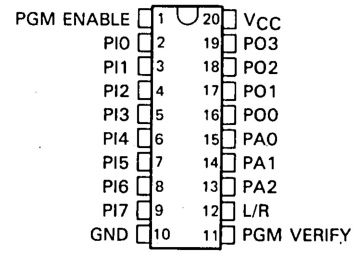
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

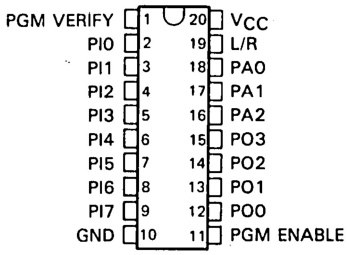
PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF, See Note 3	16	25		18	25		MHz
t_{pd}	I, I/O,	O, I/O			25	40		25	35	ns
t_{pd}	CLK↑	Q			11	35		11	25	ns
t_{en}	$\overline{OE}$↓	Q			20	35		20	25	ns
t_{dis}	$\overline{OE}$↑	Q			11	30		11	20	ns
t_{en}	I, I/O	O, I/O			25	40		25	35	ns
t_{dis}	I, I/O	O, I/O			25	35		25	30	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



Pin assignments in programming mode (PGM ENABLE, pin 1 or 11, at V_{IHH})

TABLE 1 — INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME								
	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2 — PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g. 10 kΩ to 5 V)

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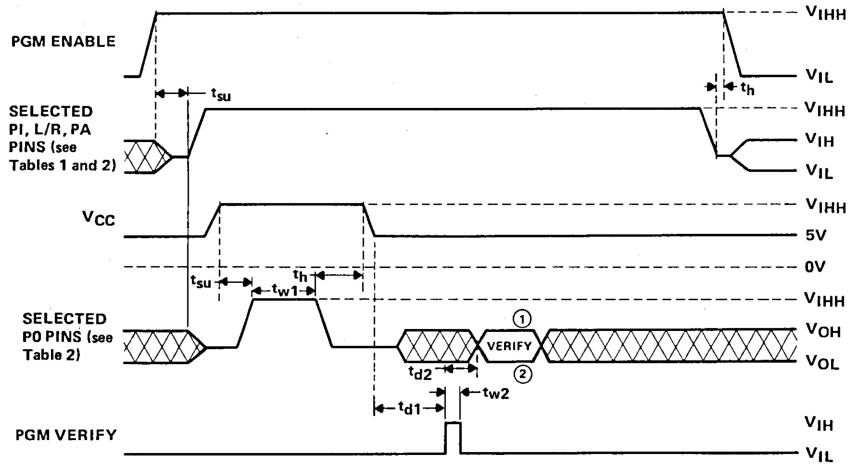
programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 32) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 Raise PGM ENABLE to V_{IHH}.
Step 2 Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 Begin selection of the output line with appropriate conditions on PA pins.
Step 4 Raise V_{CC} to V_{IHH}.
Step 5 Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6 Return V_{CC} to 5 volts and pulse PGM Verify. The PO pin selected in Step 5 will be less than V_{OL} if the fuse is open.

Steps 1 through 6 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than four times. Verification is possible only with the verify-protect fuse intact.

programming waveforms



① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

security fuse programming