TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY — TIBPAL16XX-10
DEVICES INCLUDED — TIBPAL16R4-10, TIBPAL16R6-10, TIBPAL16R8-10, and TIBPAL16L8-10

PROGRAMMING PROCEDURE:

Array fuses are programmed by executing the following programming sequence. Each fuse can be opened by selecting the appropriate (1 of 32) Input Line and (1 of 8) Product Line. The levels for selecting Input Lines and Product Lines are shown in Tables 1-2 and 1-3.

Step 1: Raise PGM ENABLE to $V_{IHH}$.
Step 2: Select an Input Line by applying appropriate levels to PI pins.
Step 3: Select a Product Line group by applying appropriate logic levels to PA pins. The actual product line selected will be determined by the PO pin (described in step 5).
Step 4: Raise /OE to $V_{IH}$.
Step 5: Raise the selected PO pin to $V_{IHH}$.
Step 6: Program the fuse by pulsing $V_{CC}$ to $V_{IHH}$.
Step 7: Remove the output voltage.
Step 8: Lower /OE to $V_{IL}$ to enable device.
Step 9: Pulse PGM VER pin to $V_{IH}$.
Step 10: Verify the blowing of fuse by checking for a $V_{OL}$ at the selected PO pin.

If the fuse is still intact, steps 1 thru 10 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed. Verification is possible only with the Security fuse intact.

A single security fuse is provided on each device to discourage the unauthorized copying of fuse patterns. To program the security fuse, follow the steps above omitting steps 5 and 10. Verification is achieved by verifying the entire fuse array. If the security fuse is blown, all other fuses will appear to be unblown.

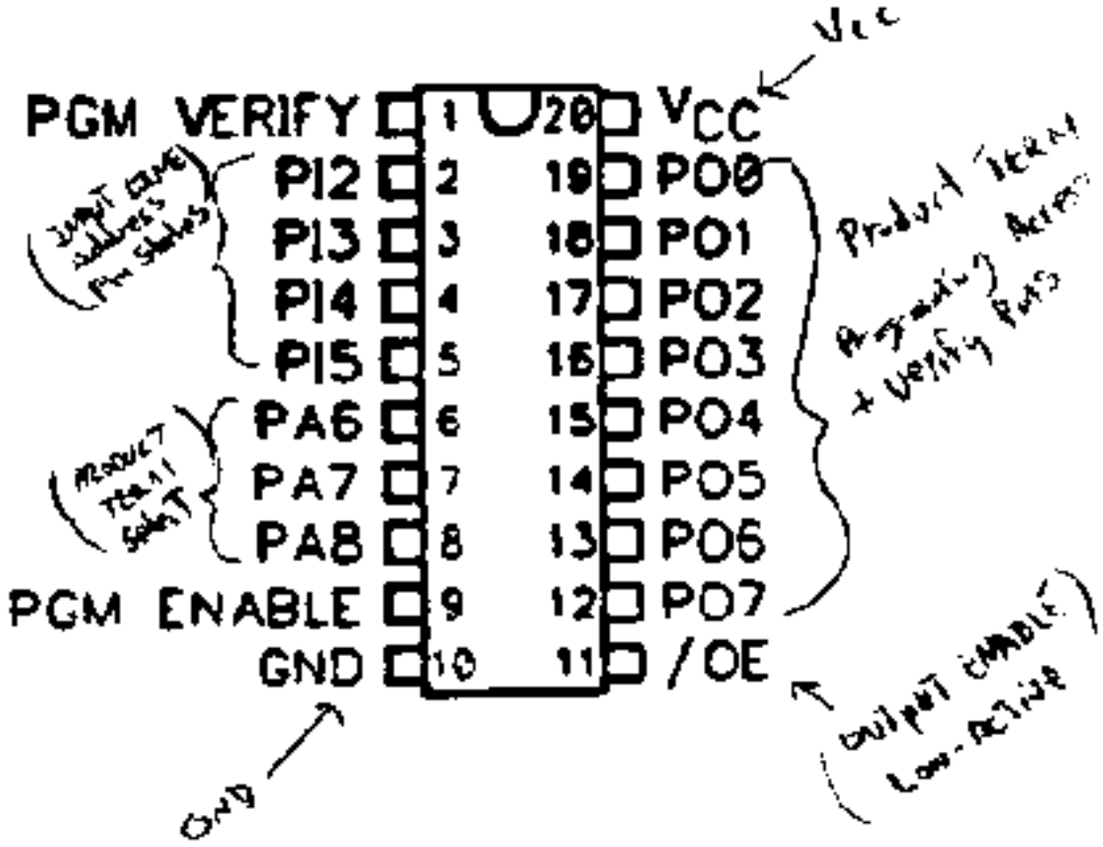
For Input and Product Line selection, see Tables 1-2 and 1-3.

For programming waveforms, see Figure 1-1.

| | | | | | |
|---|---|---|---|---|---|
| PREPARED BY: B. Cole PAL20Y-1.DWG | DATE: 12/04/86 | TEXAS INSTRUMENTS | | | |
| CHECKED BY: [signature] | DATE: 6/30/88 | TITLE: ALGORITHM SPECIFICATION TIBPAL16XX-10 | | | |
| ENGINEER: Joel Skellie | DATE: 12/04/86 | | | | |
| APPROVED BY: [signature] | DATE: 06/30/88 | REVISION: D (LETTER) | A (SIZE) | PAL20003 | SHEET: 1/10 |
| RELEASED BY | DATE: / / | | | | |

## PIN ASSIGNMENTS IN PROGRAMMING MODE

(TOP VIEW)




(TOP VIEW)

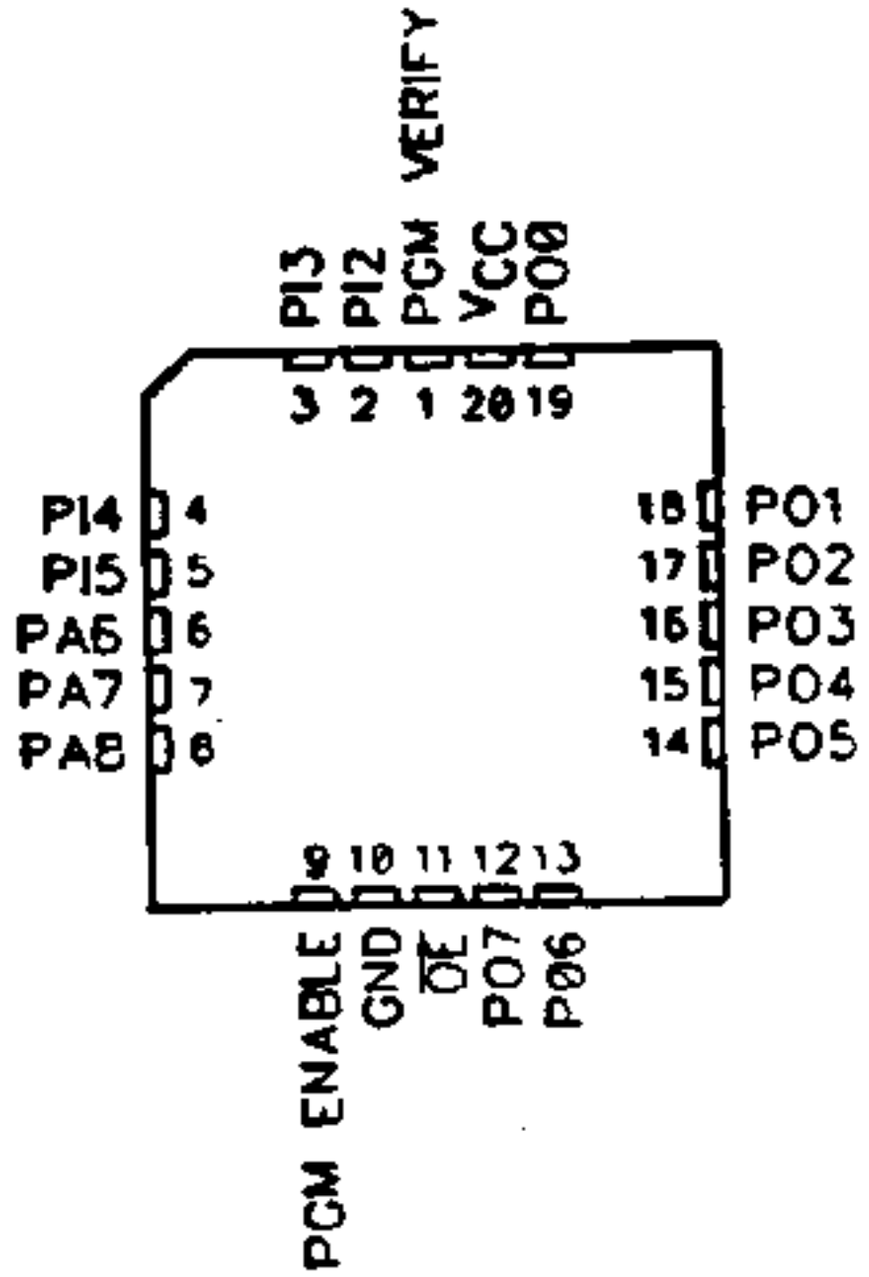



TABLE 1–1, PROGRAMMING PARAMETERS, TA = 25°C

| PARAM | DESCRIPTION | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Verify–level supply voltage | | 5.25 | 5.50 | 5.75 | V |
| $V_{IH}$ | High–Level input voltage | | 2.40 | | 5.50 | V |
| $V_{IL}$ | Low–level input voltage | | | | 0.50 | V |
| $V_{IHH}$ | Program–pulse voltage | P0 | 10.25 | 10.50 | 10.75 | V |
| | | PGM ENA | 10.25 | 10.50 | 10.75 | V |
| | | P1, PA | 10.25 | 10.50 | 10.75 | V |
| | | $V_{CC}$ | 9.5 | 9.75 | 10 | V |
| $I_{IHH}$ | Program–pulse current | P0 | | 20 | 40 | ma |
| | | PGM ENA | | 5 | 15 | ma |
| | | P1, PA | | 2 | 10 | ma |
| | | $I_{CC}$ | | | 450 | ma |
| $t_{w1}$ | Program–pulse duration at $V_{CC}$ | | 10 | | 50 | us |
| $t_{w2}$ | Pulse duration at PGM VERIFY | | 100 | | | ns |
| $t_{su}$ | Set–up time | | 100 | | | ns |
| $t_h$ | Hold time | | 100 | | | ns |
| $t_{d1}$ | Delay time from /OE low to PGM VERIFY high. | | 100 | | | ns |
| $t_{d2}$ | Delay time from PGM VERIFY high to valid output. | | 100 | | | ns |

TABLE 1–2, INPUT LINE SELECT

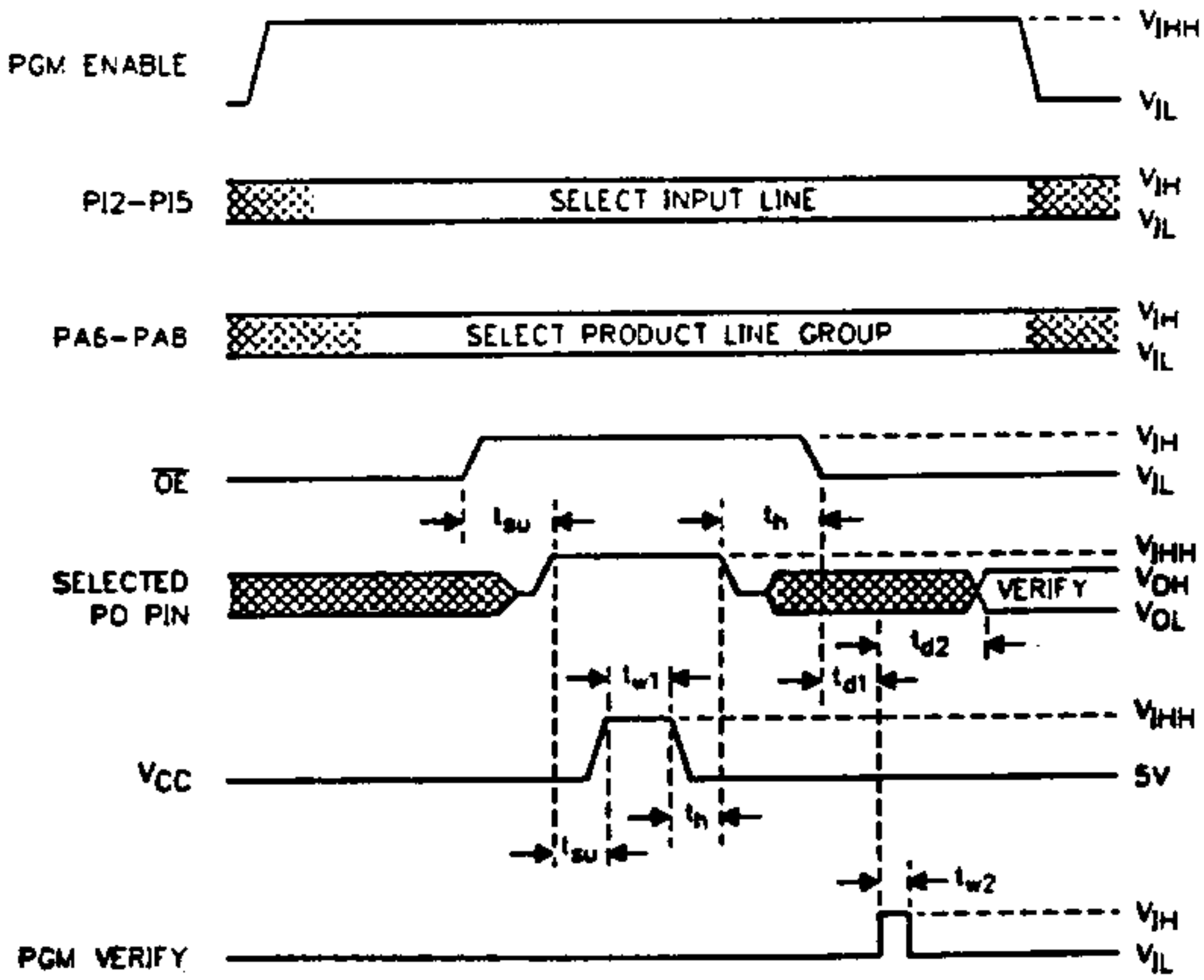
| Input Line Number | Input Line Number–Address Pin States | | | |
|---|---|---|---|---|
| | P15 | P14 | P13 | P12 |
| 00 | L | L | L | L |
| 01 | L | L | L | H |
| 02 | L | L | H | L |
| 03 | L | L | H | H |
| 04 | L | H | L | L |
| 05 | L | H | L | H |
| 06 | L | H | H | L |
| 07 | L | H | H | H |
| 08 | H | L | L | L |
| 09 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |
| 16 | H | L | L | L |
| 17 | H | L | L | H |
| 18 | H | L | H | L |
| 19 | H | L | H | H |
| 20 | H | H | L | L |
| 21 | H | H | L | H |
| 22 | H | H | H | L |
| 23 | H | H | H | H |
| 24 | L | H | L | L |
| 25 | L | H | L | H |
| 26 | L | H | H | L |
| 27 | L | H | H | H |
| 28 | H | H | L | L |
| 29 | H | H | L | H |
| 30 | H | H | H | L |
| 31 | H | H | H | H |
| SF | H | H | H | H |

TABLE 1–3. PRODUCT TERM ADDRESSING

| PRODUCT TERM | | | | | | | | Product Term Select Address Pin States | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | PA8 | PA7 | PA6 |
| 0 | 8 | 16 | 24 | 32 | 40 | 48 | 56 | L | L | L |
| 1 | 9 | 17 | 25 | 33 | 41 | 49 | 57 | L | L | H |
| 2 | 10 | 18 | 26 | 34 | 42 | 50 | 58 | L | H | L |
| 3 | 11 | 19 | 27 | 35 | 43 | 51 | 59 | L | H | H |
| 4 | 12 | 20 | 28 | 36 | 44 | 52 | 60 | H | L | L |
| 5 | 13 | 21 | 29 | 37 | 45 | 53 | 61 | H | L | H |
| 6 | 14 | 22 | 30 | 38 | 46 | 54 | 62 | H | H | L |
| 7 | 15 | 23 | 31 | 39 | 47 | 55 | 63 | H | H | H |
| SF → -- | -- | -- | -- | -- | -- | -- | -- | X | X | HH ← SF |
| P00 | P01 | P02 | P03 | P04 | P05 | P06 | P07 | L = $V_{IL}$, HH = $V_{IHH}$<br>H = $V_{IH}$ | | |
| Programming Access and Verify Pin | | | | | | | | | | |

SF – Security Fuse (Does not require voltage to the PO pin)

FIGURE 1–1. PROGRAMMING WAVEFORMS

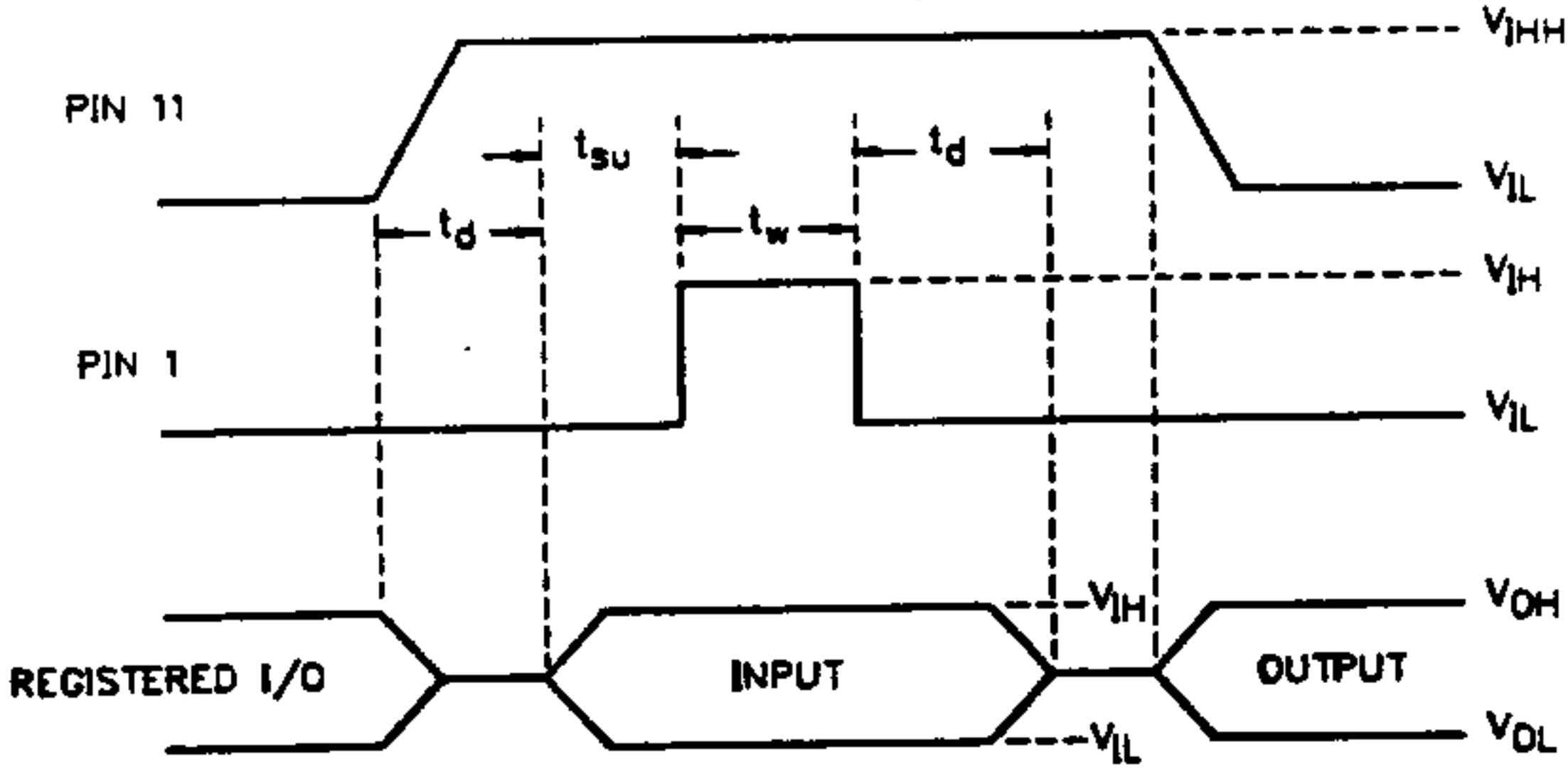


Preload procedure for registered outputs (See Note 2)

The output registers of the TIBPAL16XX–10 can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state–machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With $V_{CC}$ at 5 volts and pin 1 at $V_{IL}$, raise pin 11 to $V_{IHH}$.
Step 2. Apply either $V_{IL}$ or $V_{IH}$ to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 11 to $V_{IL}$. Preload can be verified by observing the voltage level at the output pin.

Preload waveforms (See Notes 2 and 3)




Notes: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w = 100$ ns to 1000 ns.
$V_{IHH} = 10.25$ V to 10.75 V.

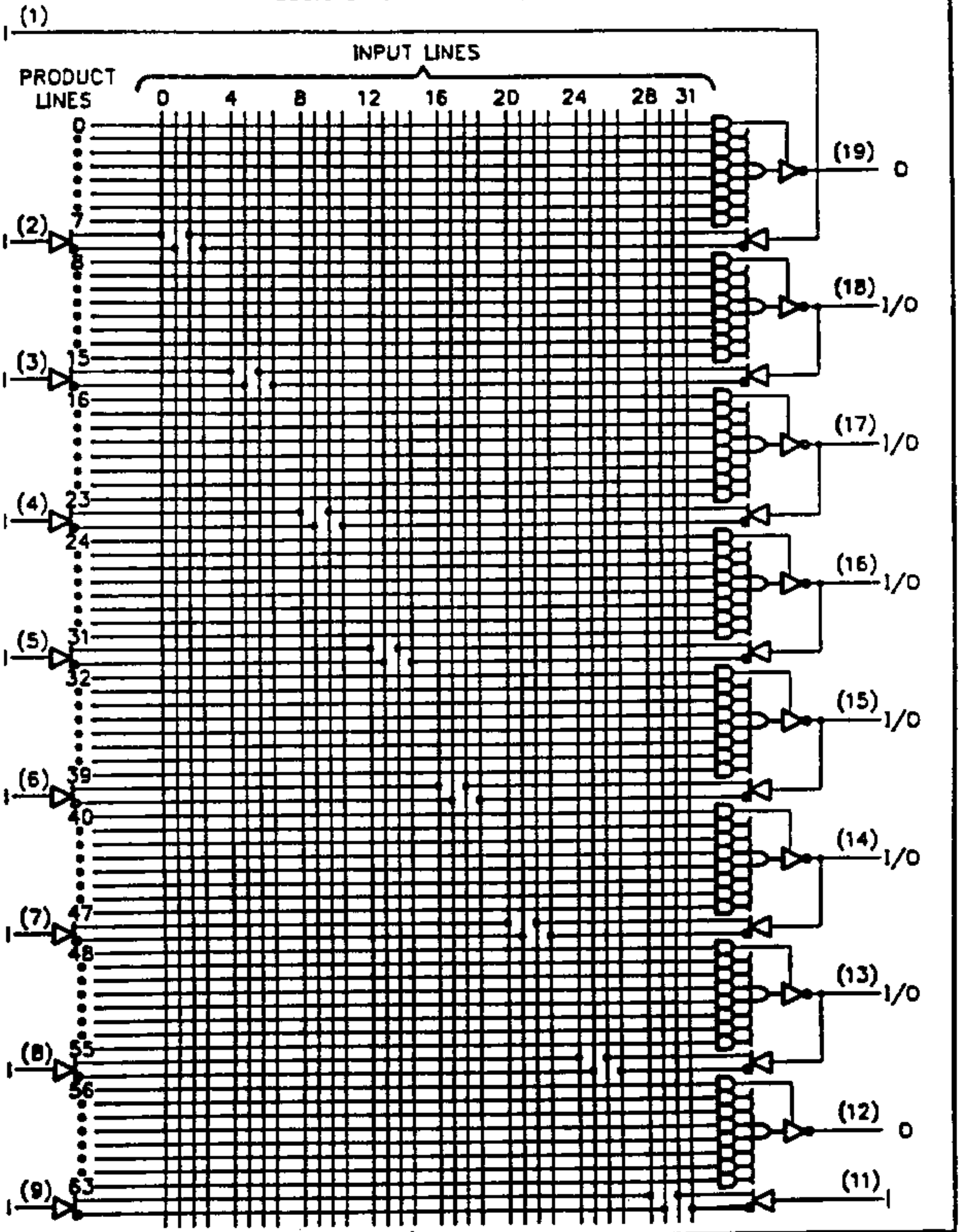
# PROGRAMMING ALGORITHM TEMPLATE

| | |
|---|---|
| SPECIFICATION NUMBER | PAL20003 |
| DEVICE FAMILY | TIBPAL16XX-10 |
| INCLUDED DEVICES | TIBPAL16L8-10, TIBPAL16R4-10, TIBPAL16R6-10, TIBPAL16R8-10 |

PROGRAMMER INFO:
MANUFACTURER : _____ MODEL: _____ ADAPTER #: _____
UPDATE VERSION : _____ FW/SW P/N: _____

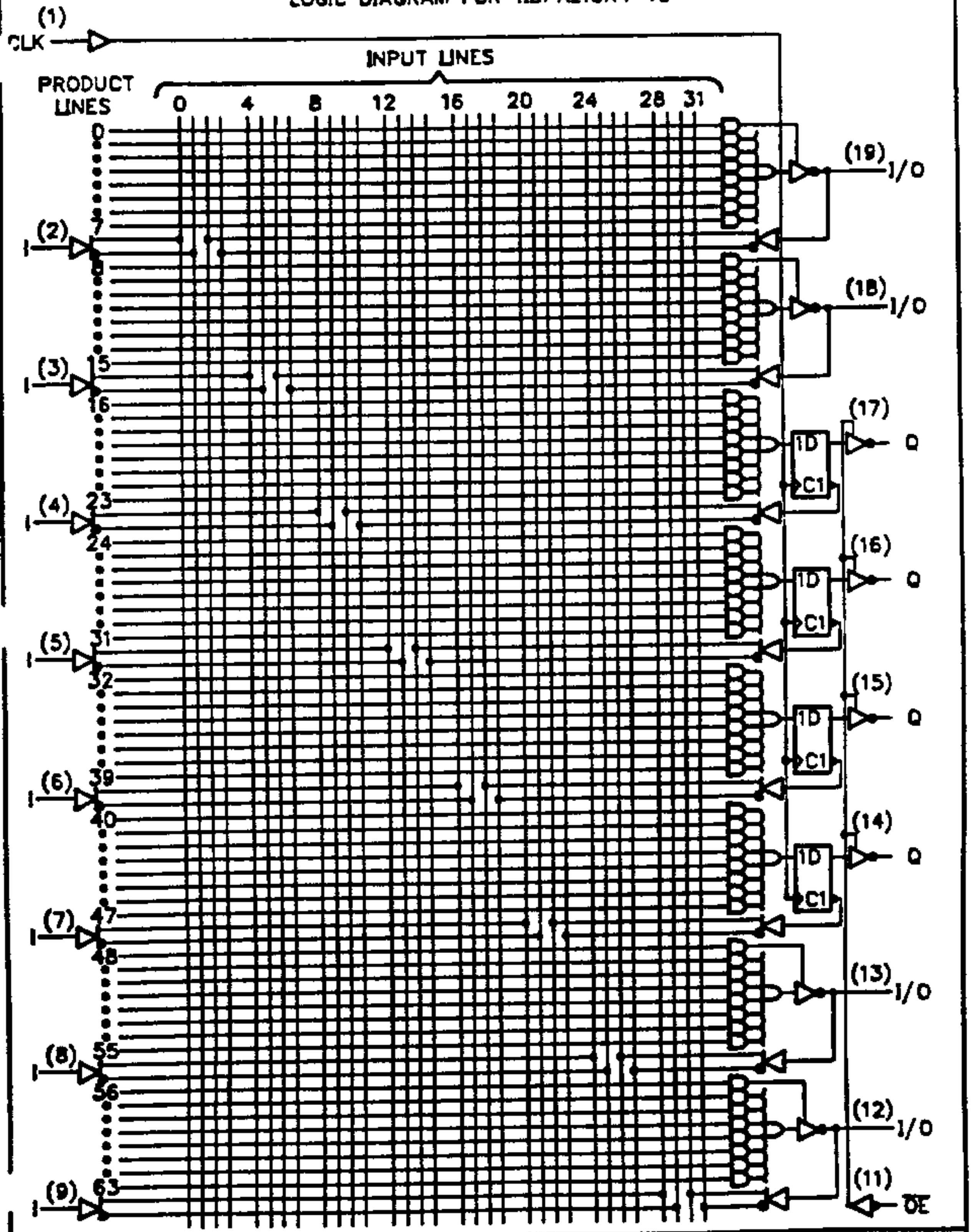
| PARAMETER | | MIN | NOM | MAX | UNITS | ACTUAL |
|---|---|---|---|---|---|---|
| VCC - VERIFY LEVEL SUPPLY VOLTAGE | | 5.25 | 5.5 | 5.75 | V | |
| VIH - HIGH LEVEL INPUT VOLTAGE | | 2.4 | | 5.5 | V | |
| VIL - LOW LEVEL INPUT VOLTAGE | | | | 0.5 | V | |
| VIHH - PROGRAM-PULSE VOLTAGE (PO PINS) | | 10.25 | 10.5 | 10.75 | V | |
| VIHH - PROGRAM-PULSE VOLTAGE (PGM ENA) | | 10.25 | 10.5 | 10.75 | V | |
| VIHH - PROGRAM-PULSE VOLTAGE (PI,PA) | | 10.25 | 10.5 | 10.75 | V | |
| VIHH - PROGRAM-PULSE VOLTAGE (VCC) | | 9.5 | 9.75 | 10.00 | V | |
| tw1 - PROGRAM PULSE WIDTH AT VCC | | 10 | | 50 | us | |
| tw2 - PGM VERIFY PULSE WIDTH | | 100 | | | ns | |
| tsu - SET UP TIME | (/OE-PO) | 100 | | | ns | |
| tsu - SET UP TIME | (PO-VCC) | 100 | | | ns | |
| th - HOLD TIME | (/OE-PO) | 100 | | | ns | |
| th - HOLD TIME | (PO-VCC) | 100 | | | ns | |
| td1 - DELAY TIME (SEE WAVEFORMS) | | 100 | | | ns | |

# LOGIC DIAGRAM FOR TIBPAL16L8-10



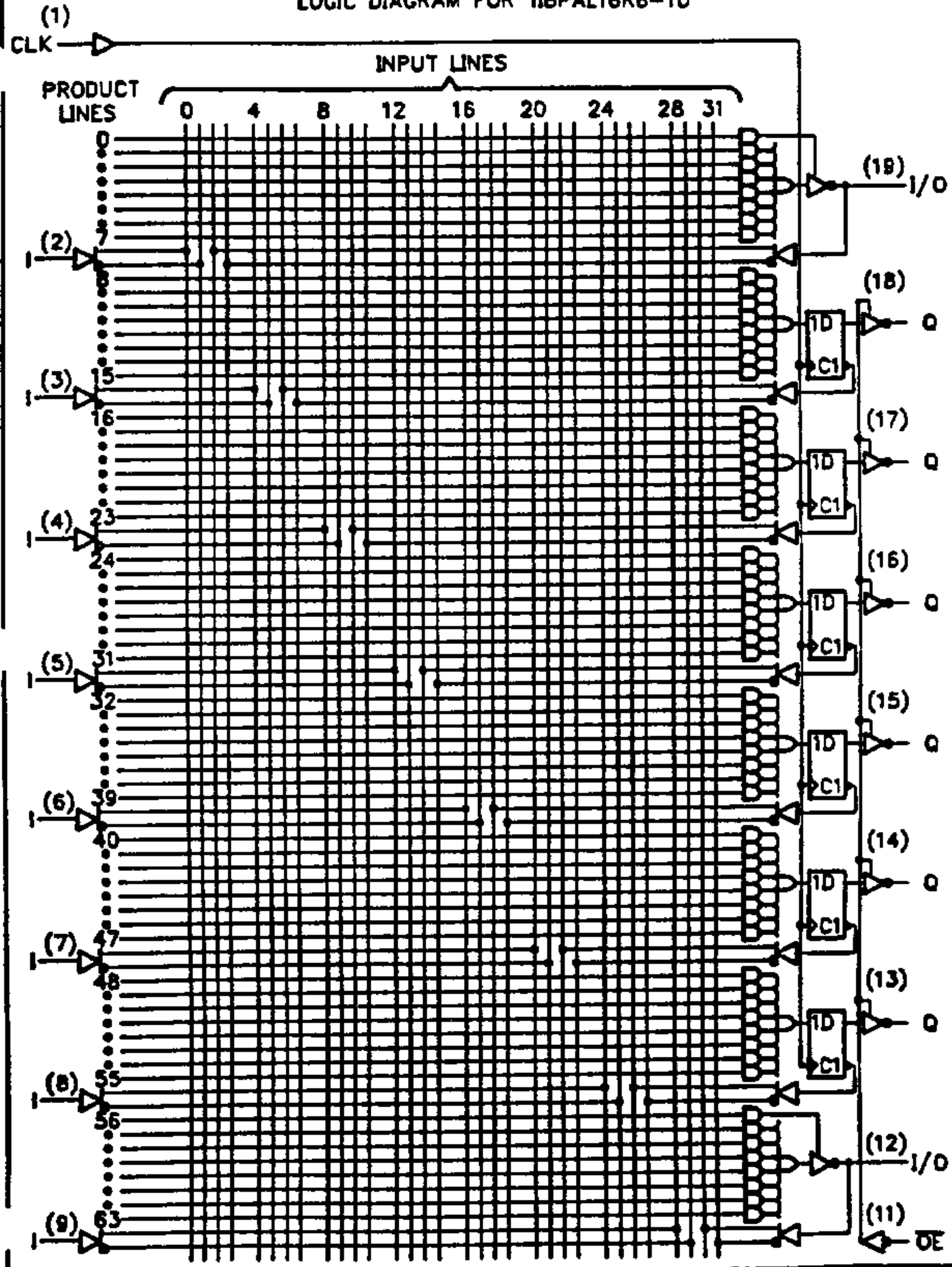

| | | | |
|---|---|---|---|
| ALGORITHM SPECIFICATION TIBPAL16XX-10 | PAL20Y-6.DWG | SH 6 of 10 | PAL20003 |

# LOGIC DIAGRAM FOR TIBPAL16R4-10



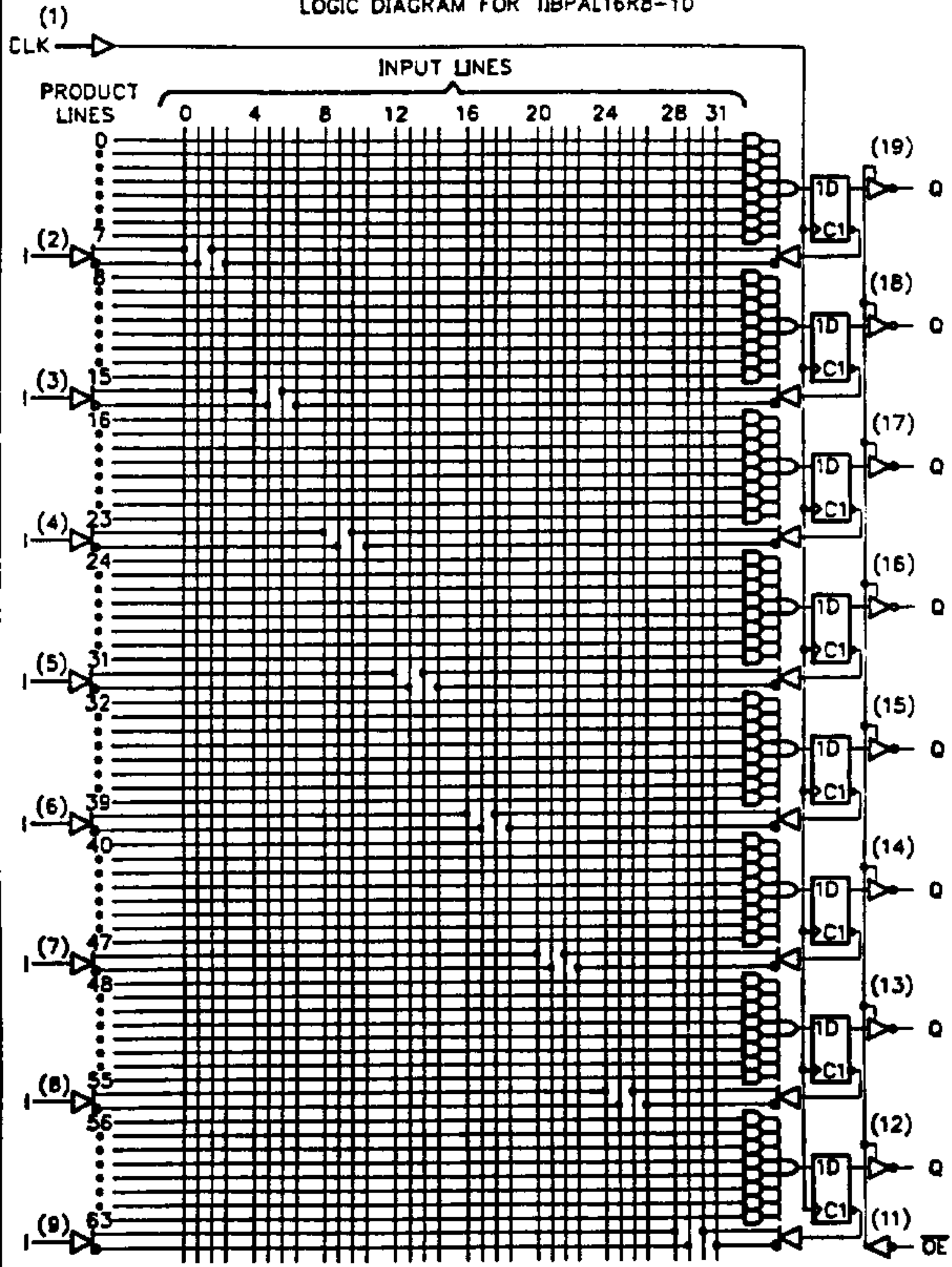

| | | | |
|---|---|---|---|
| ALGORITHM SPECIFICATION TIBPAL16XX-10 | PAL20Y-7.DWG | SH 7 of 10 | PAL20003 |

# LOGIC DIAGRAM FOR TIBPAL16R6-10




| | | | |
|---|---|---|---|
| ALGORITHM SPECIFICATION TIBPAL16XX-10 | PAL20Y-8.DWG | SH 8 of 10 | PAL20003 |

# LOGIC DIAGRAM FOR TIBPAL16R8-10




| | | | |
|---|---|---|---|
| ALGORITHM SPECIFICATION TIBPAL16XX-10 | PAL20Y-9.DWG | SH 9 of 10 | PAL20003 |

# REVISION HISTORY

| REVISION LTR. | DATE | ENGINEER | DESCRIPTION OF CHANGES |
|---|---|---|---|
| A | 06-87 | Thomas | Sheet 1 of 9. Changed Security Fuse Programming Procedure.<br>Table 1-3. Deleted the requirement for P00 pulse during security fuse programming. |
| B | 12-87 | Thomas | Changed $V_{CC}$ to Min = 5.25 V, Nom = 5.50 V, Max = 5.75 V. |
| C | 03-88 | Thomas | Added PLCC Pinout.<br>Chg. P0 to $V_{CC}$ for $t_{w1}$.<br>Chg. units from us to ns for $t_{w2}$.<br>Chg. P10-P14 to P12-P15 and PA0-PA3 to PA6-PA8. Sht. 4. |
| D | 06-88 | Thomas | Sht. 2 - chonged $t_{d2}$ units from us to ns |