THE ABI DIGITAL IC TESTER

PRODUCT DESCRIPTION

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Introduction:

The Digital IC Tester is a low cost instrument with the capability of performing a functional test on most digital IC's from the TTL (74 series), CMOS (4000 series), memory and interface device families. The entire functionality of each device supported (pinout, truth table, function table etc.) is contained within the instrument, so that the user need only know the device number to perform the test. Indeed, using the CHIP SEARCH feature even the type number may be omitted if desired as the instrument is capable of automatically determining the IC type and carrying out the appropriate test. This document contains a brief description of the operation of the instrument to enable you to understand the basic principles involved.

Hardware:

The instrument is designed around a Z80A 8 bit microprocessor, along with dedicated LSI IC's to control the keyboard and display and handle the input/output of information from the device under test. The circuit board contains provision for 2 off 27128 EPROMS to be fitted, thus giving a program capacity of 32k. At the time of writing about 3k of this capacity is unused, so that a considerable margin exists for the support of additional devices in the future. The device under test is inserted into one of four Zero Insertion Force sockets on the front panel, each pin of which can be configured, under control of the microprocessor, as an input or output to suit the device under test. The 5V supply to the sockets is applied to the usual pins (0v - bottom left, 5V - top right) via a relay that allows the sockets to be powered down under microprocessor control. The test device supply is current limited at 500mA and is independent from the main instrument 5V supply. The outputs from the instrument to the device are current limited both to prevent damage to the tester from a faulty device and also to detect grossly excessive device input current. In addition, this feature is used to check that TRI-STATE and OPEN-COLLECTOR device outputs have assumed their proper high impedance conditions. The inputs to the instrument are recognized as logical 0's if below 0.8 volts, or logical 1's if above 2 volts. Input voltages inbetween this range are undefined. Each pin of each socket is connected to the corresponding pin of the other sockets (where possible), so that the signals on a device under test may be viewed on an oscilloscope by monitoring the corresponding pin(s) on one of the unused sockets. Finally, each pin has a resistor network to provide a light load for the device under test and to ensure that unused pins assume a logical 1 state.

Software:

The first stage in testing a device is to enter the device number on the keypad, followed by the green START key to activate the test sequence for the device. At the start of each test all the pins on the instrument are set to inputs, and the test power supply relay is switched on. After a short delay to allow the power supply to stabilise, the test sequence can begin. Working from the device type number entered by the operator, the instrument next configures the pins as inputs or outputs to suit the device under test, and outputs the appropriate sequence of signals to fully exercise the device, monitoring the device outputs and checking them against the expected outputs as given in the device truth/function tables.

In the case of the simpler devices with 2 or more identical independent circuits in the same package, all possible combinations of the device inputs are used during the test, even though this means that any one gate in the package may be tested several times with the same inputs applied. This is necessary to ensure that the gates are infact independent from each other, and that for example there is no interaction between an input of one gate with the input of another. A moments consideration will reveal that this type of fault will not be detected if each gate in the package is tested independently. This method of testing means that, perhaps surprisingly, the simpler devices take longer to test than the more complex MSI and LSI devices.

With clocked devices such as flip-flops, latches, counters, shift-registers etc., the test sequence is designed to take the device through all its possible states, the instrument issuing clock, clear, load, preset etc. pulses as appropriate. A binary counter, for example, is tested by first clearing it and checking that the outputs are all low, then loading it and checking that the outputs follow suit. The counter is then cleared again and clocked through all its 16 states, the outputs being checked at each stage for the correct count. When the count reaches 15, the carry or cascade output is checked in addition. Finally, the count disable, if present, is checked for correct operation. If the counter is of the up/down type, the above sequence is repeated for the down count. The exact sequence of course varies depending on the device, but the general principles remain the same. Every feature of the device operation is thoroughly tested, both to ensure valid results and to enable the unit to correctly identify devices with only minute differences. The test sequence used for a particular device can be viewed on an oscilloscope by setting the instrument into loop mode.

Devices with TRI-STATE or OPEN-COLLECTOR outputs are first of all tested for functionality using the principles outlined above, then the device inputs are configured such that the device outputs assume the high impedance state. The instrument then re-configures the pins connected to the outputs of the device under test and checks that these outputs are infact floating and can be pulled high and low.

Memory devices are tested using an algorithm that results in all combinations of logical 0's and 1's being written into each cell in the device, to fully exercise all locations in the package. To check for multiple addressing, the entire memory is filled with a pattern calculated from the address and a modifier, then read back and checked. This process is then repeated with a new modifier. The address, data and control signals are all generated by the instrument according to the device type number. With the byte wide static ram devices (eg. 6116) this test takes a considerable time, so an option is included to cut down the number of patterns used to reduce this time. The result is dramatic improvement in throughput, at the expense of a slightly less rigorous test. Since most faults are gross functional failures, this shortened test will still find the majority of faulty devices.

Interface devices cover a wide range of varying types of device, including line drivers and receivers, peripheral power drivers, bus transceivers, timers, opto-isolators etc.. The basic principles outlined above apply equally to these devices. Some devices in this family are not included because they require multiple supply voltages or have non-digital inputs. The range of devices supported represents an attempt to cover the most popular from a vast range, so if the device you use is not listed, please enquire.

Some of the devices supported by the instrument have non-standard power supply pins, and a header must be used to enable these devices to be tested as described in the operators manual. Most of these devices have been superseded and replaced by equivalents with the power supply pins in the standard position, but the software is provided for those still using these devices. In addition certain other devices require headers to be fully tested, including monostable devices and 8 pin peripheral drivers from the interface family.

In addition to the basic test method described above, the instrument has test loop facilities which are described fully in the operators manual. One feature worthy of mention here however is the CHIP SEARCH mode, which enables the instrument to automatically determine the type of device inserted by searching through its entire range of devices. The device, having been identified, is tested and the results displayed in the usual way, so that a "mixed bag" of devices can be quickly sorted out into good and bad devices without having to read the type number of each device. There will be certain ambiguities in the outcome of the search in some cases due to pin compatibility of devices with similar functions but differing type numbers. Devices which require headers to be tested as described in the device lists in the operators manual will only be identified if the correct header is present when the search is performed.

General:

The basic philosophy behind the design of the instrument is that by far the majority of faulty devices are found to be gross functional failures, as opposed to slight changes in AC and DC specifications. For example, one major manufacturer published a reliability report that shows the percentage changes in parameters such as Vil, Vih, Voh, Vol, were less than 1% of their initial value over a 1000 hour test at 125 degrees C. This means that provided the devices were within the manufacturers specification when shipped, they will almost certainly remain within this specification during their useful life. This principle means that provided one can test the functionality of a device, quickly and at low cost, one can be reasonably confident that a functional device is infact within the manufacturers specification. This principle applies even more so in environments such as R & D laboratories, workshops and educational establishments, where it is quite likely that faulty devices have been subject to varying levels of accidental misuse, so that they are almost certain to be functional failures.

A.B.I. are always striving to improve the range of devices covered by the instrument. If you have any particular requirement that is not covered at the present time, or any comment or query about the operation of the instrument, please do not hesitate to contact Ian Fletcher on (0226) 751639.