Signetics

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Status	Product Specification
Programmable Logic Devices	

PLHS18P8A/B

PAL®-Type Devices

DESCRIPTION

The PLHS18P8A and the PLHS18P8B are two-level logic elements consisting of 72 AND gates and 8 OR gates with fusible connections for programming I/O polarity and direction.

All AND gates are linked to 10 inputs (I) and 8 bidirectional I/O lines (B). These yield variable I/O gate configurations via 8 direction control gates, ranging from 18 inputs to 8 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates. The 72 AND gates are separated into 8 groups of 9 each. Each group of 9 is associated with one bidirectional pin. In each group, eight of the AND terms are ORed together, while the ninth is used to establish I/O direction. All outputs are individually programmable via an Ex–OR gate to allow implementation of AND/OR or NAND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

The PLHS18P8A/B is field-programmable, allowing the user to quickly generate custom patterns using standard programming equipment.

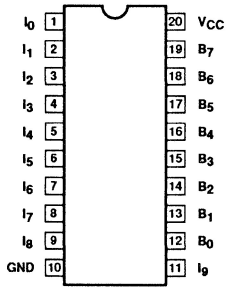
Order codes are listed in the Ordering Information Table.

FEATURES

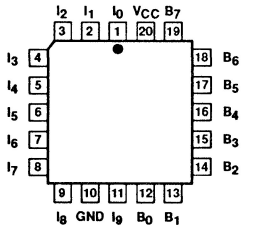
- **"A" version 100% functionally compatible with AmPAL18P8A and all 16L8, 16P8, 16H8, 16L2, 16H2, 14L4, 14H4, 12L6, 12H6, 10L8, 10H8, 16LD8 and 16HD8 "A" speed PAL-type products**
- **"B" version 100% functionally compatible with AmPAL18P8B and all 16L8, 16P8, 16H8, 16L2, 16H2, 14L4, 14H4, 12L6, 12H6, 10L8, 10H8, 16LD8 and 16HD8 "B" speed PAL-type products**
- **Field-programmable**
- **10 inputs**
- **8 bidirectional I/O lines**
- **72 AND gates/product terms**
  - **configured into eight groups of nine**
- **Programmable output polarity (3-State output)**
- **I/O propagation delay:**
  - **PLHS18P8A: 20ns (max)**
  - **PLHS18P8B: 15ns (max)**
- **Power dissipation: 500mW (typ)**
- **TTL compatible**
- **Security fuse**

PIN CONFIGURATIONS

N Package



A Package



APPLICATIONS

- **100% functional replacement for all 20-pin combinatorial PAL devices**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

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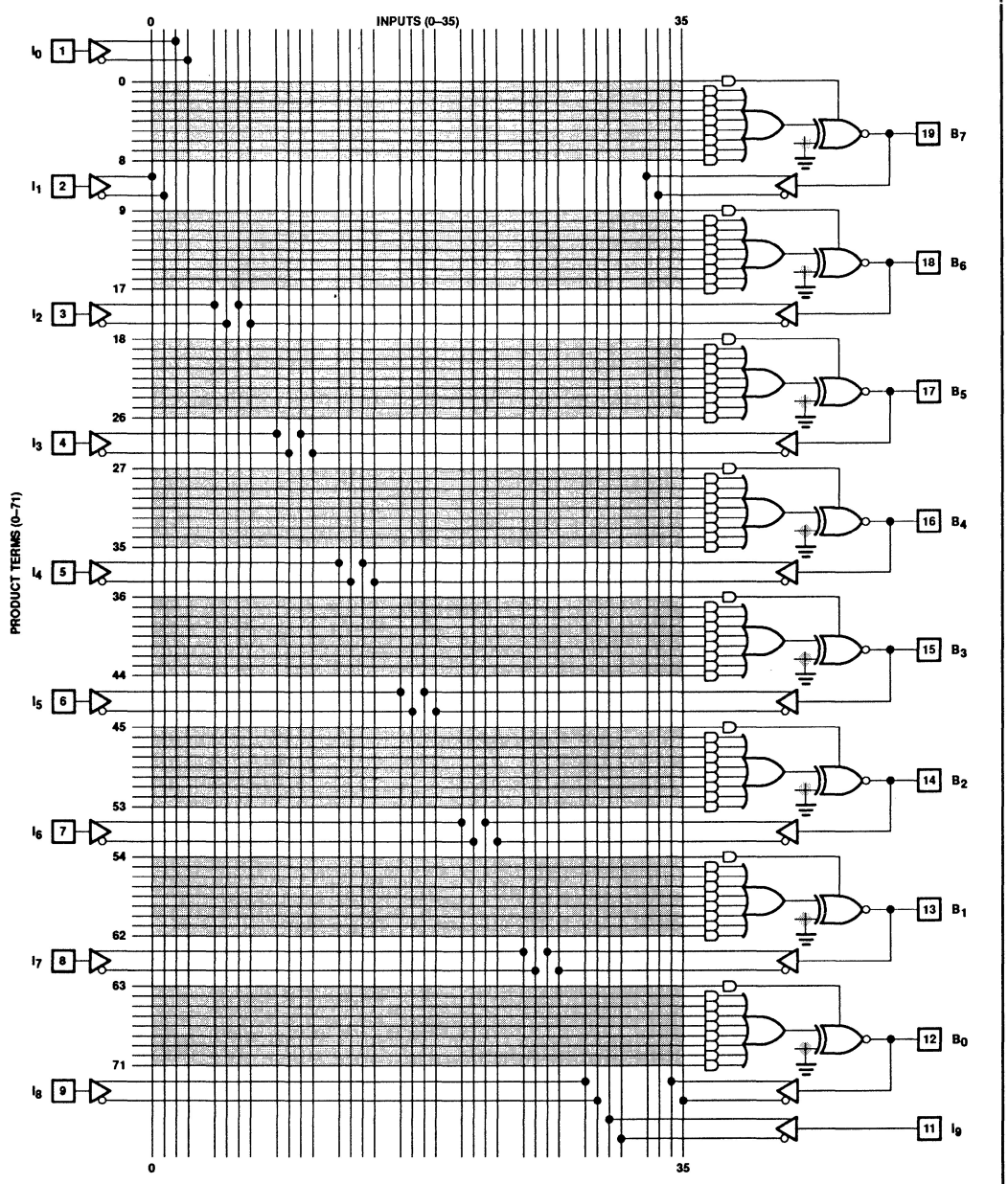
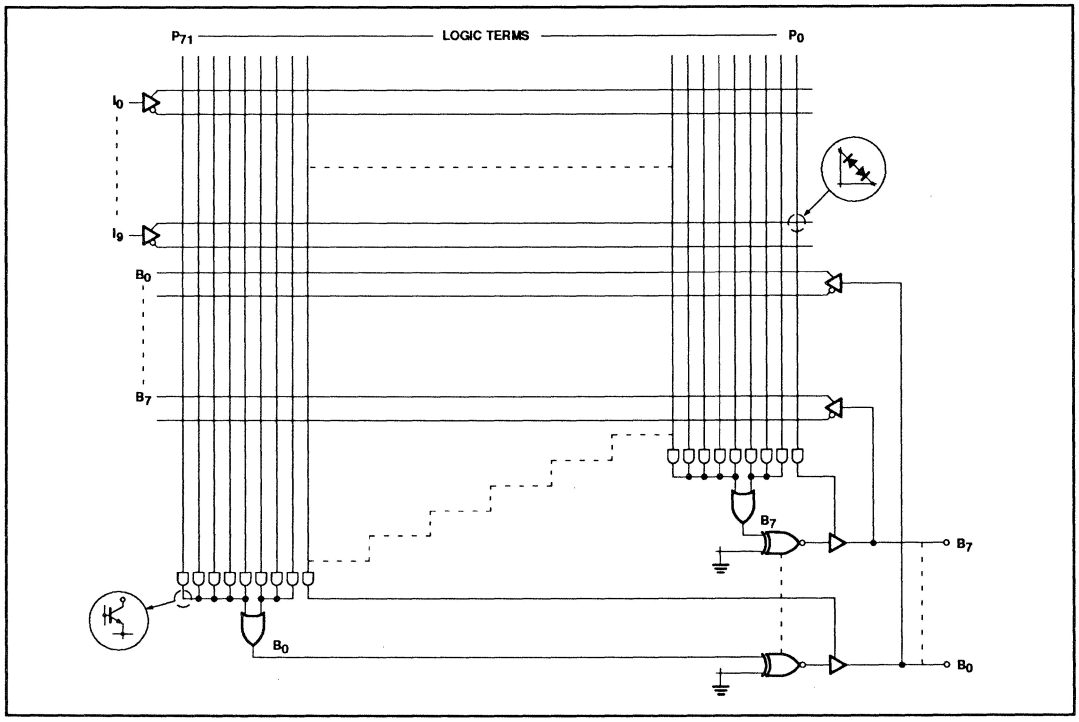
FPLA LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. ▒ Programmable connections.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20–Pin Plastic Dual In–Line (300mil-wide)	PLHS18P8AN, PLHS18P8BN
20–Pin Plastic Leaded Chip Carrier	PLHS18P8AA, PLHS18P8BA

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +7	V_{DC}
V_{IN}	Input voltage	–0.5 to +5.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} Max	V_{DC}
V_{OUTPRG}	Output voltage (programming)	+21	V_{DC}
I_{IN}	Input current	–30 to +5	mA
I_{OUT}	Output current	+100	mA
I_{OUTPRG}	Output current (programming)	+170	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–65 to +150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			PLHS18P8A			PLHS18P8B			
			Min	Typ[1]	Max	Min	Typ[1]	Max	
Input voltage[2]									
V_{IL}	Low	V_{CC} = MIN			+0.8			+0.8	V
V_{IH}	High	V_{CC} = MAX	+2.0			+2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = −18mA		−0.9	−1.2		−0.9	−1.2	V
Output voltage									
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}							
V_{OL}	Low	I_{OL} = +24mA			+0.50			+0.50	V
V_{OH}	High	I_{OH} = −3.2mA	+2.4	+3.5		+2.4	+3.5		V
Input current									
		V_{CC} = MAX							
I_{IL}	Low	V_{IN} = +0.40V		−20	−100		−20	−100	µA
I_{IH}	High	V_{IN} = +2.7V			+25			+25	µA
I_I	High	V_{IN} = +5.5V			+1.0			+1.0	mA
Output current									
		V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2.0V							
I_{OZH}	Output leakage	V_{OUT} = +2.7V			+100			+100	µA
I_{OZL}	Output leakage	V_{OUT} = +0.40V			−250			−250	µA
I_{OS}	Short circuit[3]	V_{OUT} = +0.5V	−25	−60	−90	−30	−60	−90	mA
I_{CC}	V_{CC} current	V_{CC} = MAX, All inputs = GND		100	155		100	155	mA
Capacitance[4]									
		V_{CC} = +5V							
C_{IN}	Input	V_{IN} = 2.0V @ f = 1MHz		6			6		pF
C_{OUT}	I/O	V_{OUT} = 2.0V @ f = 1MHz		9			9		pF

NOTES:

1. Typical limits are at V_{CC} = 5.0V and T_A = +25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. These parameters are not 100% tested, but are periodically sampled.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 200\Omega$, $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITIONS	LIMITS						UNIT
					PLHS18P8A			PLHS18P8B			
					Min	Typ	Max	Min	Typ	Max	
t_{PD}	Propagation delay	Output ±	Input ±	$C_L = 50pF$		14	20		12	15	ns
t_{EA}	Output enable	Output –	Input ±	$C_L = 50pF$		14	20		12	15	ns
t_{ER}	Output disable	Output +	Input ±	$C_L = 5pF$		14	20		12	15	ns

NOTES:
1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = +25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For 3–State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high–impedance to High tests and closed for high–impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High–to–High impedance tests are made to an output voltage of $V_{OH} = -0.5V$ with S_1 open, and Low–to–High impedance tests are made to the $V_{OL} = +0.5V$ level with S_1 closed.

VIRGIN STATE

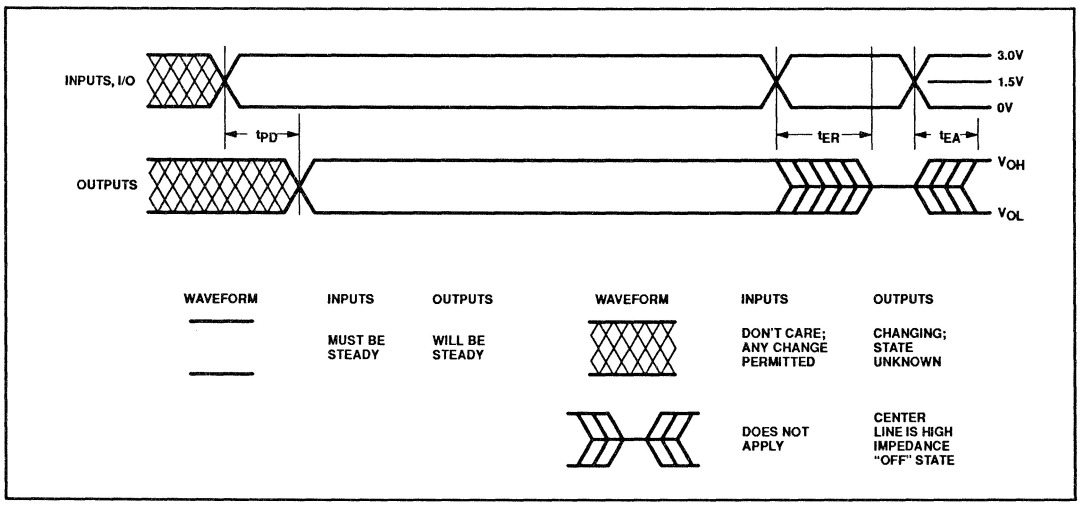
A factory shipped virgin device contains all fusible links open, such that:

1. All outputs are at "H" polarity.
2. All outputs are enabled.
3. All p–terms are enabled.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Input to output propagation delay.
t_{ER}	Input to output disable (3–State) delay (Output Disable).
t_{EA}	Input to Output Enable delay (Output Enable).

TIMING DIAGRAM



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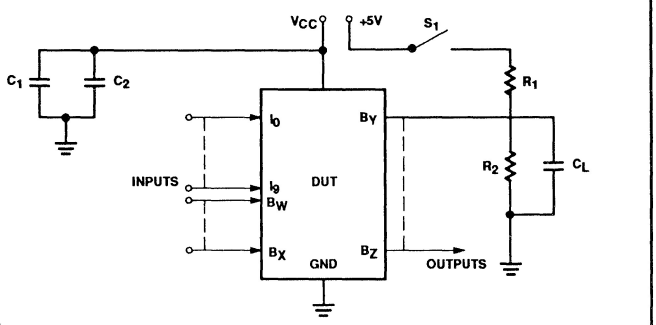
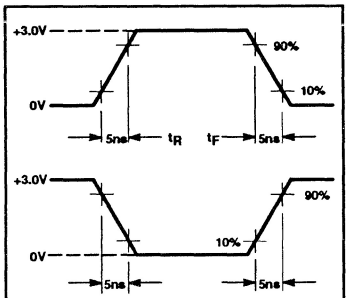
AC TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

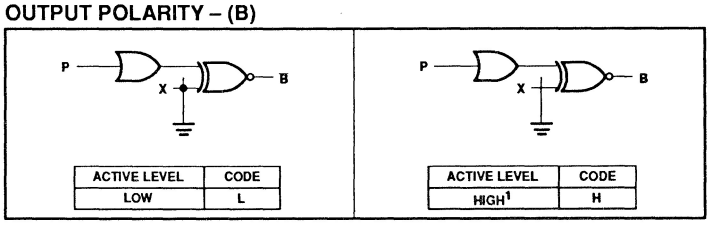
LOGIC PROGRAMMING

PLHS18P8A/B logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLHS18P8A/B logic designs can also be generated using the program table format detailed on the following pages. This program table entry (PTE) format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

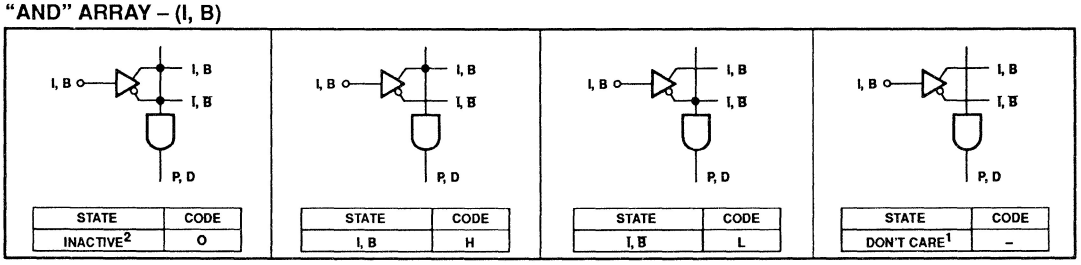
OUTPUT POLARITY – (B)



ACTIVE LEVEL	CODE
LOW	L

ACTIVE LEVEL	CODE
HIGH[1]	H

"AND" ARRAY – (I, B)



STATE	CODE
INACTIVE[2]	O

STATE	CODE
I, B	H

STATE	CODE
I, B	L

STATE	CODE
DON'T CARE[1]	-

NOTE:
1. This is the initial state of all link pairs.
2. All unused product terms must be programmed with all pairs of fuses in the INACTIVE state (all fuses on an unused p–term must be programmed).

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PROGRAM TABLE