PLS173

DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement (I, B) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

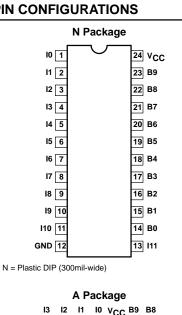
Order codes for this device are listed below.

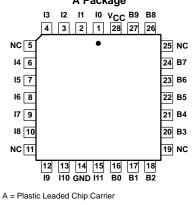
FEATURES

- I/O propagation delay: 30ns (max.)
- 12 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active-High or -Low outputs
- 42 product terms:
 - 32 logic terms
 - 10 control terms
- Ni-Cr programmable links
- Input loading: -100µA (max.)
- Power dissipation: 750mW (typ.)
- 3-State outputs
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing





ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Dual-In-Line 300mil-wide	PLS173N	0410D
28-Pin Plastic Leaded Chip Carrier	PLS173A	0401F

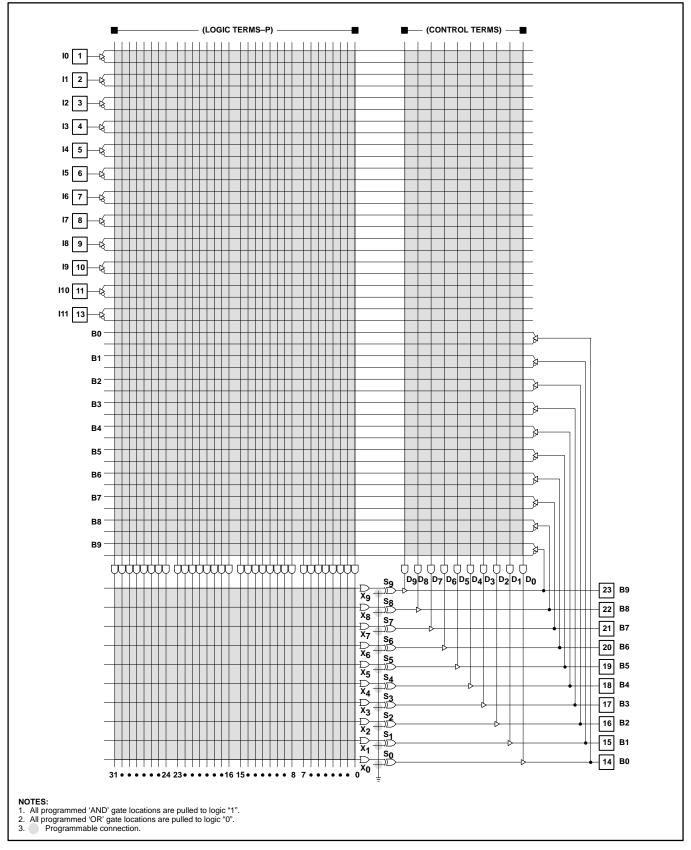
PIN CONFIGURATIONS

Programmable logic array $(22 \times 42 \times 10)$

Product specification

```
PLS173
```

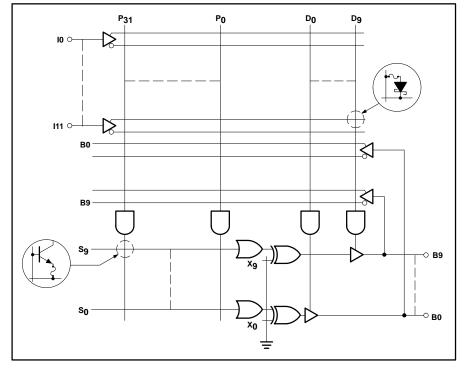
LOGIC DIAGRAM



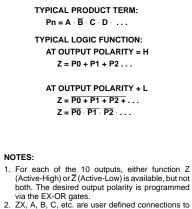
Programmable logic array $(22 \times 42 \times 10)$

PLS173

FUNCTIONAL DIAGRAM



LOGIC FUNCTION



 ZX, A, B, C, etc. are user defined connections to fixed inputs (I), and bidirectional pins (B).

ABSOLUTE MAXIMUM RATINGS¹

		RAT		
SYMBOL	PARAMETER	Min	Max	UNIT
V _{CC}	Supply voltage		+7	V _{DC}
V _{IN}	Input voltage		+5.5	V _{DC}
V _{OUT}	Output voltage		+5.5	V _{DC}
I _{IN}	Input currents	-30	+30	mA
I _{OUT}	Output currents		+100	mA
T _{amb}	Operating free-air temperature range	0	+75	°C
T _{stg}	Storage temperature range	-65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS173 is also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Philips Semiconductors Military Data Handbook.

PLS173

Product specification

DC ELECTRICAL CHARACTERISTICS

 $0^{\circ}C \leq T_{amb} \leq \text{+}75^{\circ}C, \ \text{4.75} \leq V_{CC} \leq 5.25V$

SYMBOL				LIMITS		
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ¹	MAX	UNIT
$\begin{tabular}{ c c c c c } \hline SYMBOL & PARAMETER & TEST CONDITIONS & MIN & TYP1 & MAX & U \\ \hline Input voltage2 & & & & & & & & & & & & & & & & & & &$						
V _{IL}	Low	V _{CC} = MIN			0.8	V
V _{IH}	High	$V_{CC} = MAX$	2.0			V
V _{IC}	Clamp ³	$V_{CC} = MIN, I_{IN} = -12mA$		-0.8	-1.2	V
Output vo	ltage ²					
		V _{CC} = MIN				
V _{OL}	Low ⁴	I _{OL} = 15mA			0.5	V
V _{OH}	High ⁵	$I_{OH} = -2mA$	2.4			V
Input curr	ent ⁹		•			
		V _{CC} = MAX				
I _{IL}	Low	V _{IN} = 0.45V			-100	μΑ
I _{IH}	High	$V_{IN} = V_{CC}$			40	μΑ
Output cu	rrent					
		$V_{CC} = MAX$				
I _{O(OFF)}	Hi-Z state ⁸	V _{OUT} = 5.5V			80	μΑ
		V _{OUT} = 0.45V			-140	
I _{OS}	Short circuit ^{3, 5, 6}	$V_{OUT} = 0V$	-15		-70	mA
I _{CC}	V _{CC} supply current ⁷	V _{CC} = MAX		150	170	mA
Capacitan	ce		-			
		$V_{CC} = 5V$				
I _{IN}	Input	V _{IN} = 2.0V		8		pF
CB	I/O	V _B = 2.0V		15		pF

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25^{\circ}C$. 2. All voltage values are with respect to network ground terminal. 3. Test one at a time.

4. Measured with inputs V_{IL} applied to I_{11} . Pins 1–5 = 0V, Pins 6–10 = 4.5V, Pin 11 = 0V and Pin 13 = 10V. 5. Same conditions as Note 4 except Pin 11 = +10V.

6. Duration of short circuit should not exceed 1 second.

7. I_{CC} is measured with I_0 and $I_1 = 0V$, and $I_2 - I_{11}$ and $B_0 - B_9 = 4.5V$. Part in Virgin State. 8. Leakage values are a combination of input and output leakage.

9. I_{IL} and I_{IH} limits are for dedicated inputs only $(I_0 - I_{11})$.

PLS173

AC ELECTRICAL CHARACTERISTICS

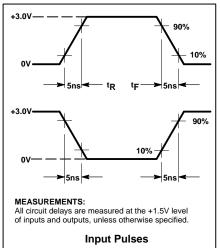
 $0^{\circ}C \le T_{amb} \le +75^{\circ}C, \ 4.75 \le V_{CC} \le 5.25V, \ R_1 = 470\Omega, \ R_2 = 1k\Omega$

				TEST		LIMITS		
SYMBOL	PARAMETER	FROM	то	CONDITION	MIN	ТҮР	MAX	UNIT
t _{PD}	Propagation delay ²	Input ±	Output ±	$C_L = 30 pF$		20	30	ns
t _{OE}	Output enable ¹	Input ±	Output –	$C_L = 30 pF$		20	30	ns
t _{OD}	Output disable ¹	Input ±	Output +	$C_L = 5pF$		20	30	ns

NOTES:

1. For 3-State output; output enable times are tested with $C_L = 30$ pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5$ pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S₁ open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S₁ closed. 2. All propagation delays are measured and specified under worst case conditions.

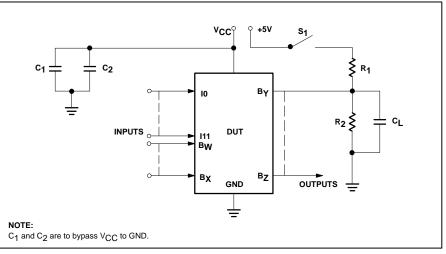
VOLTAGE WAVEFORM



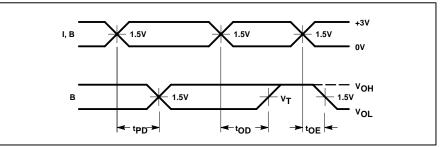
TIMING DEFINITIONS

SYMBOL	PARAMETER
t _{PD}	Propagation delay between input and output.
t _{OD}	Delay between input change and when output is off (Hi-Z or High).
t _{OE}	Delay between input change and when output reflects specified output level.

TEST LOAD CIRCUIT



TIMING DIAGRAM



Programmable logic array $(22 \times 42 \times 10)$

PLS173

LOGIC PROGRAMMING

The PLS173 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP, Data I/O Corporation's ABEL™, and Logical Devices Incorporated's CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS173 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Philips Semiconductors SNAP PLD design software package.

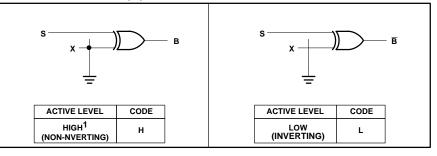
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

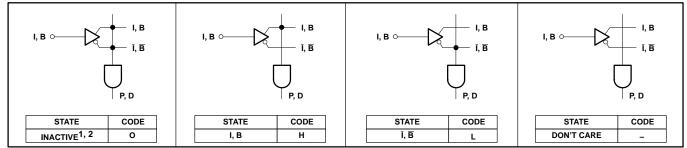
AND ARRAY - (I, B)

PROGRAMMING AND SOFTWARE SUPPORT

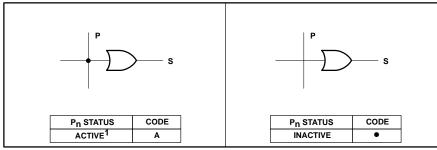
Refer to Section 9 (Development Software) and Section 10 (Third-Party Programmer/Software Support) of this data handbook for addtional information.

OUTPUT POLARITY – (B)





OR ARRAY - (B)



VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

- 1. All outputs are at "H" polarity.
- 2. All Pn terms are disabled.
- 3. All Pn terms are active on all outputs.

NOTES:

- 1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n , D_n . Any gate P_n , D_n will be unconditionally inhibited if both the True and Complement of any input
- 2. (I, B) are left intact.

ABEL is a trademark of Data I/O Corp.

CUPL is a trademark of Logical Devices, Inc.

PROGRAM TABLE

																									_	_	_				RITY			
		T E											A	ND											L					OR				
		R						1											B(I)										B(0))			
		М	11	10	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	· (6	5	4	3	2	1
		0																									Ţ				ļ			
	щ	1																									Ţ							
	DATE	2																									1							
		3																							_		+	+	1		t	-		
	>	4																			\vdash		-			+	+	+	+	-	t	+	+	-
	REV	5						-	_	-						_					\vdash		-	-	_	+	+	+	+		+	-	+	-+
		6					_	-	_	-						_				_	\vdash		-	_		-	+	+	+	-	+		+	-
	**	7					_	_		_						_					\vdash		_	_	_	-	+	-	+	-	+		+	_
<u>ب</u> #	Ë.	8					_	_		_						_							_	_		-	+	-	_	_	+	_	_	\rightarrow
CE A	BL							_		_													_	_	_		+	_	_		-	_	_	_
Z Š	TA	9																						_			1							
Ë E	M	10																																
S S	R/	11																																
ST ILII	90	12																									Í				_ĺ		_1	
CUSTOMER NAME PHILIPS DEVICE #	PROGRAM TABLE #	13																									Î	T	T	T	Ĩ			
	_	14																									Í				i			
		15						-													\vdash		+				Í	+	+	+	i	+	+	+
τ g g	5	16				1		+		Ì										ĺ	\vdash		+	\neg		1	Ť	+	+	+	i	+	+	+
 NOTES The PLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table. (Shown BLANK for clarity.) Unused Land R bits in the AND array must be procremend. 		17								-1						-				- 1	\vdash			_		-	i	-	+		i		-	
ckgr ists		18					_	_		-1						-					\vdash		-	_		+	i	-	+		i	-	-	-
bac s ex	2014	19					_	_		-1						-				_	\vdash		_	_		-	i	+	+	-	-i	_	_	\rightarrow
us a he								_		1						_				_	\vdash		_	_		-	÷	_	_	_	-i	_		\rightarrow
gin Thu	, inst	20				ļ				_i						_								_			÷	_			_			
of vii	Don't Care (—). Don't Care (—). Unused product terms can be left blank.	21				Ĺ				_i						_								_			i_							
tes of arr	eft t	22								Ĺ																	1							
link stat	pel	23				Í				İ						Ì				Ĭ							ł							
hal g to ity.)	can	24				Í				İ																	i				ł			
d wit ndin clar	sm:	25				Í				Ī																	i				i			
spol spol	t tel	26				Í				ĺ										Ĭ							ł							
orre ship	n () pq	27				i				-i										i							ł				ł			
TES The PLA is shipped with all of entries corresponding to table. (Shown BLANK for clarity.)	Don't Care (—). Unused product	28				-i				—i						-								-			+	+	+	-	-	-	+	-
e PL entric own sec	it C usec	29				li		_	_	—i						-1							-	_	_	+	÷	+	+		-	-	+	-
The PL of entri (Showr Unused	Unu Unu	30				li	_	_		—i						-							-	_	_	+	+	+	+		-	-	+	-+
¥÷ °	i ri	31				l i		_		—i						_							_	_	_	-	+	_	+	_	-		_	_
						L-i		_		—i						_				_														
		D9				L i				_i						_								_k						T	T	T	T	T
B(0)	(POL)	D8				Li																		_!)									
	e)	D7)									
: <u> </u>	гг	D6)									
ACTIVE INACTIVE CONTRO	Ξz	D5																						Т)									
	HIGH	D4																					-	T)									
		D3																					+	ľ)									
1 I I		D2														_								ĸ										
1 1 1 L L L L L L L L		D1					_			-				-								_		-K										
1		D0					_	-		-i						_				_			_	-K										
			42	44	40		_	-	6	-	4	2	2	4	22	22	24	20	40	40	47	40	45	4.4	1.00			4 0	0		40	47	10	45
		PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14		22	2 2'	1 2	U 1	19 '	18	17 1	10	15
· · · · · · · · · · · · · · · · · · ·																																		
	1	щ																																
	DON'T CARE	VARIABLE NAME																																
INACTIVE	U L	AN A																																
	NO	I₹∠																																
L B B	ā	[
			1	.				- 1				.									1			1		1	1		1					- 1

PLS173

POLARITY

Programmable logic array $(22 \times 42 \times 10)$

PLS173

SNAP RESOURCE SUMMARY DESIGNATIONS

