Latches and flip-flops with PLS153 AN014

DESCRIPTION

Using the simple AND, OR and INVERT logic functions of the PLS153, memory functions such as latches and edge-triggered flip-flops may be implemented with a relatively small part of the chip and without external wiring. In this application note, we will discuss the implementation of two R-S latches, a D-latch, an edge-triggered R-S flip-flop, an edge-triggered D flip-flop, and an edge-triggered JK flip-flop.

SIMPLE R-S LATCH

A simple R-S latch may be formed by cross-coupling two NAND functions together as shown in Figure 1.

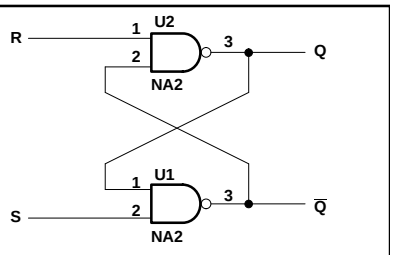


Figure 1. RS Latch

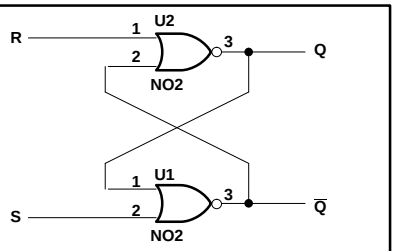


Figure 3. RS Latch

```
@pinlist
r      i;
s      i;
q      b;
qn     b;
@logic equations
qn = (/q*/s);
q = (/r*/qn);
qn . oe = 1;
q . oe = 1;
```

Figure 4. RS Latch SNAP Equations

```
@pinlist
r      i;
s      i;
q      b;
qn     b;

@logic equations
qn = /(q*s);
q = /(r*qn);
qn . oe = 1;
q . oe = 1;
```

Figure 2. RS Latch SNAP Equations

ANOTHER SIMPLE R-S LATCH

Another way to implement a simple latch is shown in Figure 3, in which two NOR functions are cross-coupled to form a latch.

The SNAP equations are shown in Figure 4.

Since each AND-term of the PLS153 can accommodate up to 18 inputs (true or inverting inputs of eight from I_0 to I_7 and ten from B_0 to B_9), and each OR circuit can be connected to up to thirty-two AND-terms, we can add additional features such as those shown in Figure 5.

The programming of this design is left to the reader as an exercise.

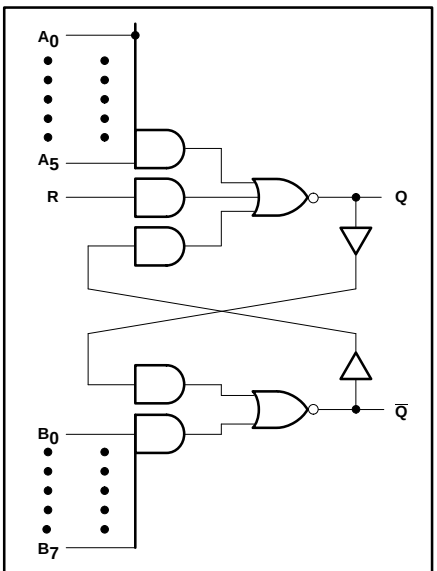


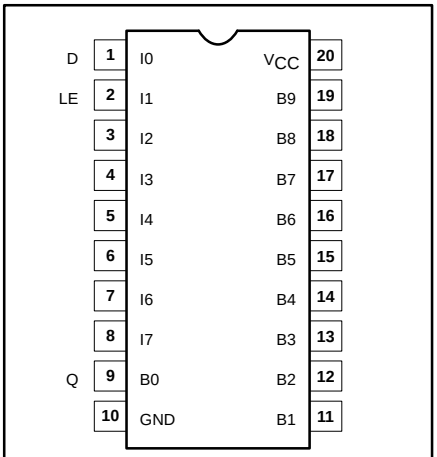
Figure 5. Expanded RS Latch

D-LATCH

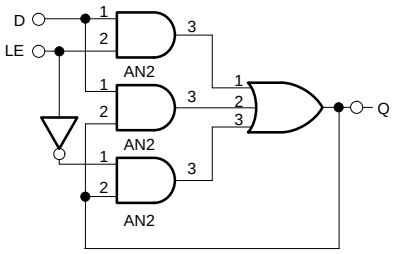
A simple D-latch can be constructed with a PLS153 as shown in Figure 6.

This circuit may be easily programmed into the PLS153 as shown in Figure 7. Note that according to the K Map of Table [1], there is a static hazard using only two gates, so the D * Q term is recommended.

This circuit may be expanded to have multiple D-latches using the same latch enable (LE).



a. Pinout



b. D-Latch Schematic

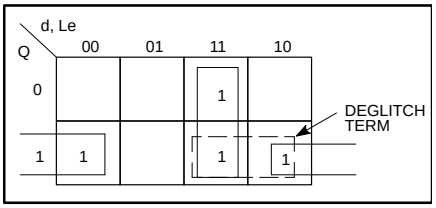
Figure 6.

```
@pinlist
d     i;
le    i;
q     o;

@logic equations
q = ((d * le)
   +  (d * q)
   +  (d * /le));
```

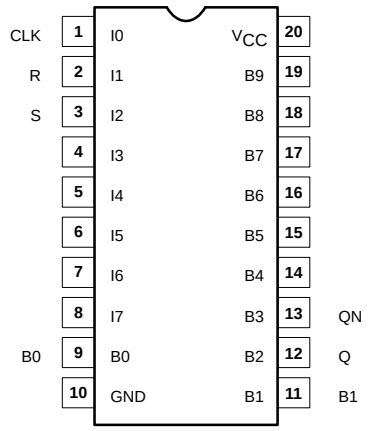
Figure 7. D– Latch SNAP Equations

Table 1. D-Latch K Map



R-S FLIP-FLOP

Two R-S latches may be combined to form a master-save flip-flop that is triggered at the rising-edge of the clock (or the falling-edge of the clock, if the designer so desires). Figure 9 shows a combination of two sets of cross-coupled NOR gates concatenated to form the flip-flop. The implementation of this circuit using SNAP equations is shown in Figure 8.



a. Pinout

@pinlist

clk i;
r i;
s i;
b0 b;
b1 b;
q b;
qn b;

@logic equations

qn = / (q
+ (b1 * clk));
q = / ((clk * b0)
+ qn);
b1 = / b0
+ (s * / clk);
b0 = / ((r * /clk)
+ b1):

b0 · oe = 1;
b1 · oe = 1;
q · oe = 1;
qn · oe = 1;

Figure 8. SNAP Equations

A PLS153 may be programmed as shown in Figure 11 to implement the D flip-flop.

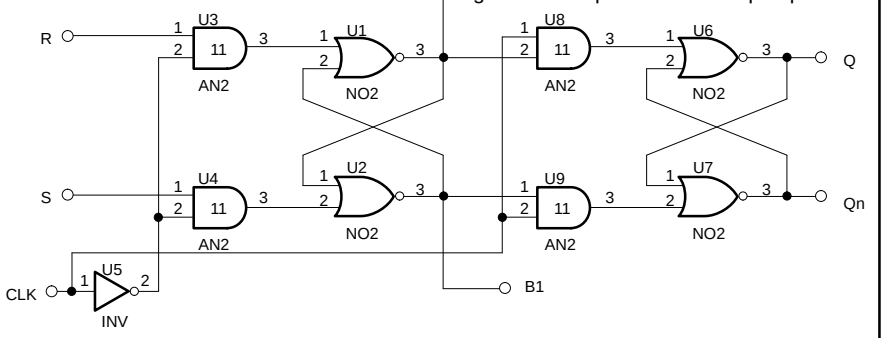


Figure 9. R-S Edge Triggered Latch

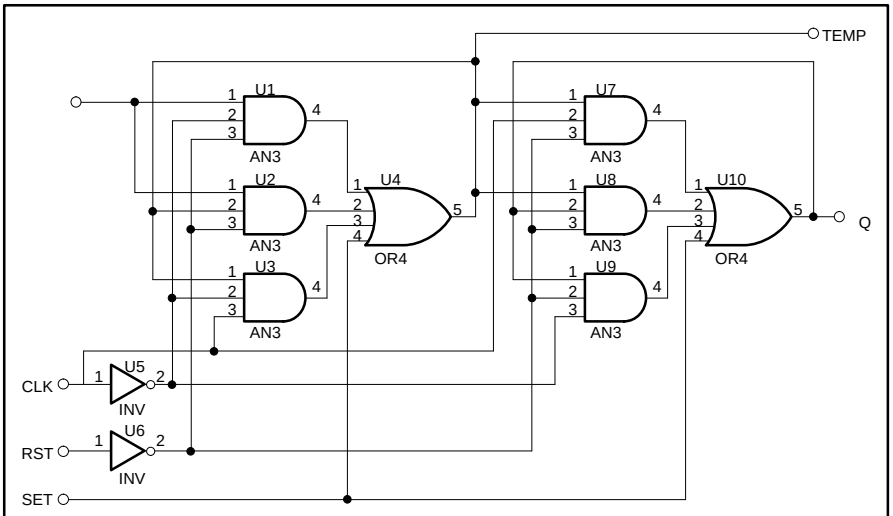
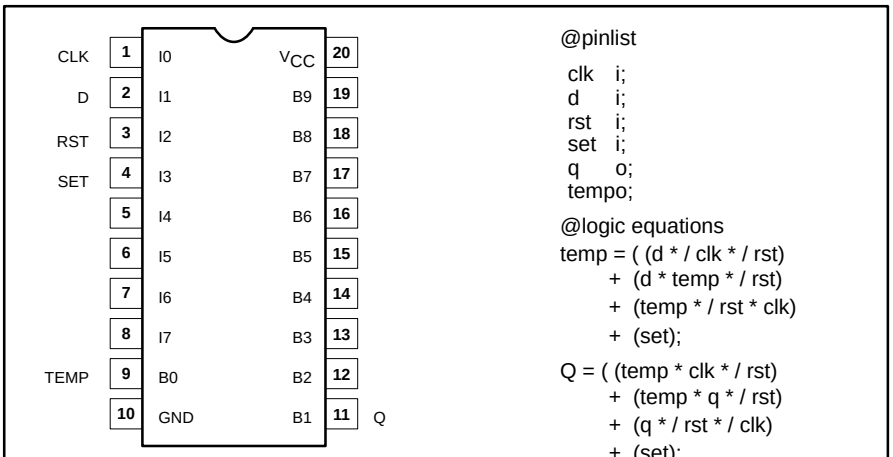


Figure 10. D-type Flip-Flop



@pinlist

clk i;
d i;
rst i;
set i;
q o;
tempo;

@logic equations

temp = ((d * / clk * / rst)
+ (d * temp * / rst)
+ (temp * / rst * clk)
+ (set);

Q = ((temp * clk * / rst)
+ (temp * q * / rst)
+ (q * / rst * / clk)
+ (set);

Figure 11. SNAP Equations and Pinout

D FLIP-FLOP

An edge-triggered master-slave D flip-flop may be constructed with two D-latches in the manner shown in Figure 10.

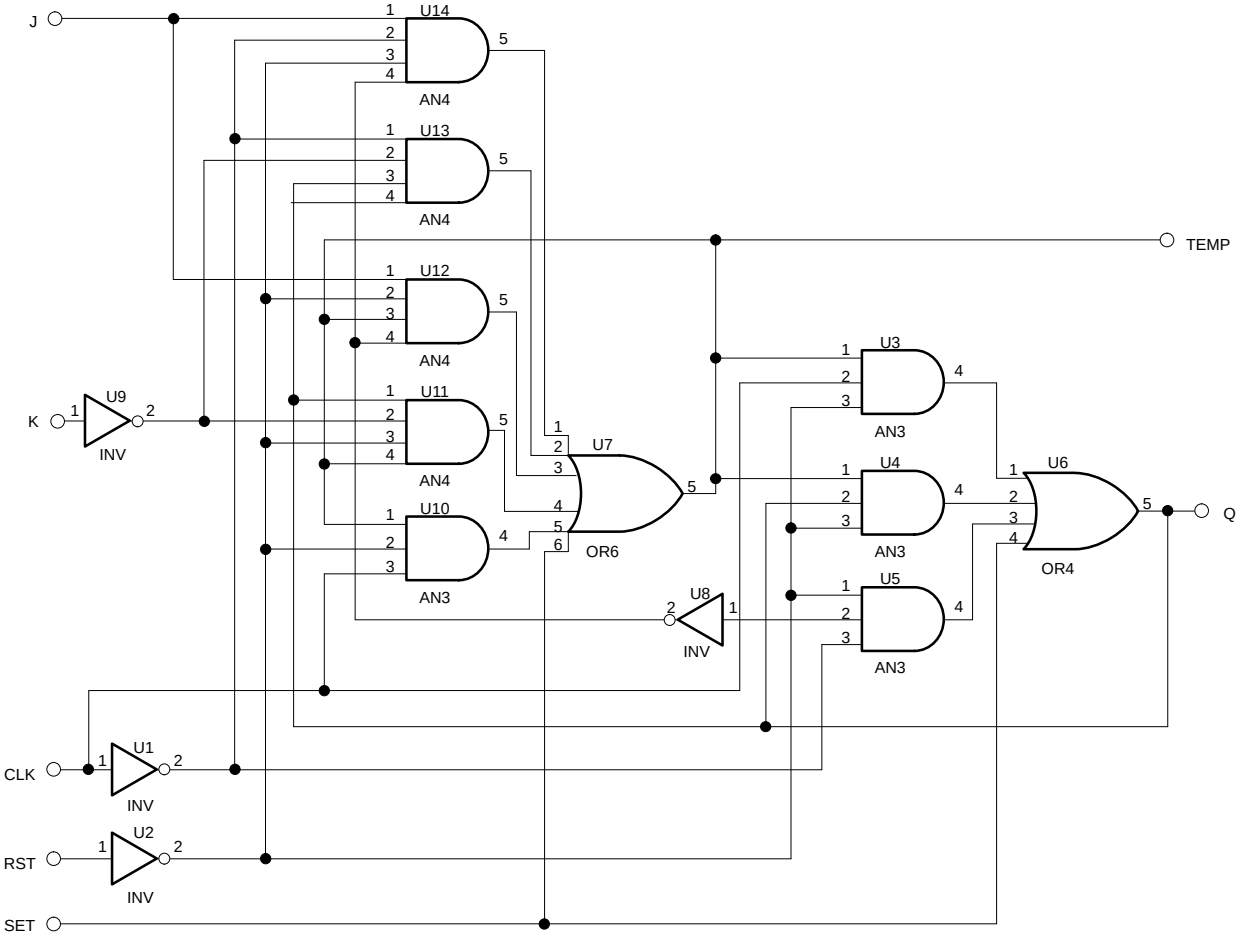
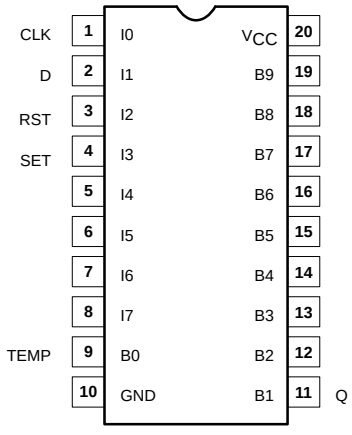


Figure 12. JK-type Flip-Flop




```
@pinlist
 clk   i;
 j     i;
 k     i;
 rst   i;
 set   i;
 q     o;
 tempo;

@logic equations
temp = ( (j * / clk * / rst * /q)
       +  (/clk * / k *q * / rst)
       +  (j * / rst * temp * /q)
       +  (temp * /rst * clk)
       +  (set);
   q = ( (temp * clk * / rst)
       +  (temp * q * / rst)
       +  ( / rst  * q * / clk)
       +  (set);
```

Figure 13. SNAP Equations and Pinout

JK FLIP-FLOP

An edge-triggered JK flip-flop schematic is shown in Figure 12. SNAP equations and pinout are shown in Figure 13.