VP16RP8M PRELIMINARY

CMOS MASK PROGRAMMABLE LOGIC ARRAY

FEATURES

- Low cost Mask Programmable Logic Array
- Pin compatible with industry standard HALs/PALs*
- Semicustom replacement for 7400 and 4000 series SSI/MSI
- Delay time—25 ns tPD max
- Operating current—45 mA max
- Complete TTL or HCMOS compatibility
- Improved testability through register pre-load
- Industry standard 300 mil 20-pin packages
- Fast prototype turnaround

DESCRIPTION

The VP16RP8M combines bipolar speed and CMOS power dissipation in a pin-compatible replacement of industry standard programmable logic arrays. Devices which may be replaced by VP16RP8M are listed in Table 1. Customer logic equations are implemented through a metal mask option to make customer specified interconnects in the AND and OR planes, rather than using the fuses or EPROM cells that are found in field programmable logic arrays. Metal is the programming medium because it is one of the last steps in the fabrication process. Thus, lead times to prototypes and production are minimized.

Through utilization of advanced CMOS processing and automated mask generation techniques, VTI has developed a design automation system to create custom masks directly from customer logic equations or programmed PALs. The VP16RP8M-25 offers designers 25 ns delay times, at up to one-third the power of the equivalent bipolar devices. VTI's VP16RP8M is compatible in all respects with the 20-pin AND and OR array structures incorporated in HAL/PAL devices and VTI's electrically erasable programmable logic device, the GAL*16V8.

PIN CONFIGURATION

VP16RP8M
VP16RP8M-25

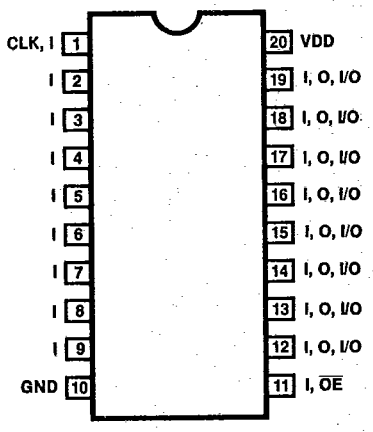

TABLE 1: REPLACEMENT GUIDE

VTI Device	Access Time	Cross Reference
VP16RP8M	35 ns	PAL10L8, PAL10H8, PAL12H6, PAL16R8, PAL12L6, PAL14H4, PAL14L4, PAL16R6, PAL16H2, PAL16L2, PAL16L8, PAL16R4, PAL16L8A-2, PAL16R6A-2, PAL16R4A-2, GAL16V8-35, VP16V8E
VP16RP8M-25	25 ns	PAL10P8, PAL12P6, PAL14P4, PAL16P2, PAL16L8A, PAL16R8A, PAL16R6A, PAL16R4A, PAL16P8A, PAL16RP8A, PAL16RP6A, PAL16RP4A, GAL16V8-25, VP16V8E-25, PAL 16L8B-2, PAL 16R8B-2, PAL 16R6B-2, PAL 16R4B-2

PIN DESCRIPTIONS

I	Input
O	Output
I/O	Transceiver
CLK	Register Clock
$\overline{OE}$	Output Enable

*HAL and PAL are registered trademarks of Monolithic Memories, Inc.
GAL is a trademark of Lattice Semiconductor Corporation.

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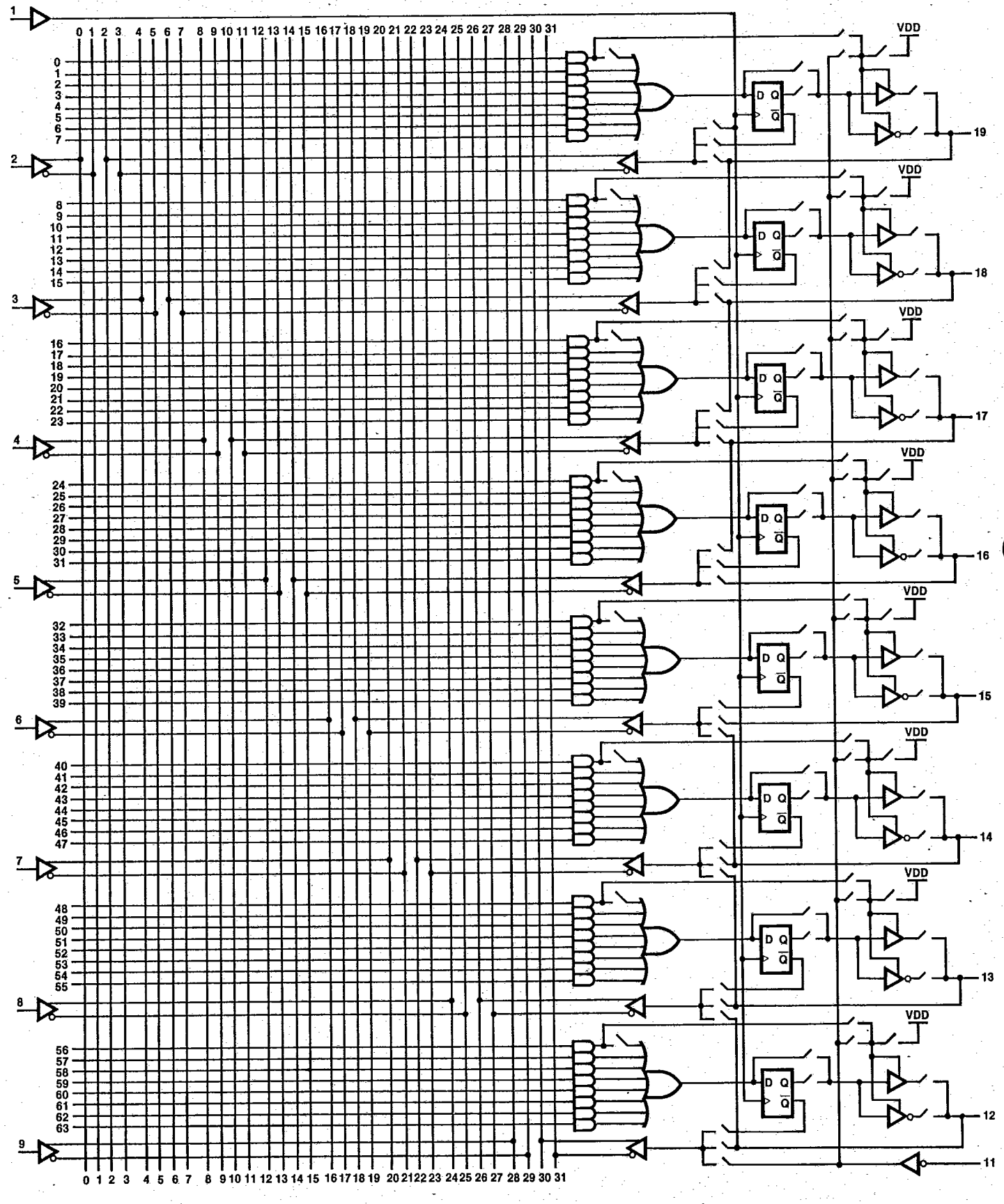
VP16RP8M PRELIMINARY

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0 to +70°C
Storage Temperature	−65 to +150°C
Supply Voltage (Referenced to VSS)	−0.3 to +6.0 V
Input Voltage on Any Pin (Referenced to VSS)	−0.3 to +6.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0 to +70°C, VDD = 5 V ±10%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VOH	Output HIGH Voltage	2.4			V	VDD = 4.50 V, IOH = −3.2 mA
		4.4			V	IOH = −20 µA
VOL	Output LOW Voltage		0.3	0.5	V	VDD = 4.50 V, IOL = 24 mA
				0.1	V	IOL = 20 µA
VIH	Input HIGH Voltage	2.0			V	
VIL	Input LOW Voltage			0.8	V	
ILI	Input Leakage Current	−20		+20	µA	VIN = VSS to VDD
ILO	Output Leakage Current	−20		+20	µA	VOUT = VSS to VDD, $\overline{OE}$ = VIH
IDD1	Supply Current VP16RP8M VP16RP8M-25			45 55	mA	VDD = 5.50 V, Inputs = 2.4 V, Note 1
IDD2	Supply Current VP16RP8M VP16RP8M-25			35 45	mA	VDD = 5.50 V, Inputs = 0 V or VDD
IDD3	Average Operating Current VP16RP8M VP16RP8M-25		20 22		mA	VDD = 5.50 V, f = 10 MHz Outputs Unloaded
IOS	Output Short-Circuit Current, Note 2	−30		−130	mA	VDD = 5.50 V

CAPACITANCE TA = 0 to +70°C, VDD = 5 V ±10%

Symbol	Parameter	Typ	Units	Conditions
CIN	Input Capacitance	5	pF	VIN = 0 V
COUT	Output Capacitance	7	pF	VOUT = 0 V

AC CHARACTERISTICS TA = 0 to +70°C, VDD = 5 V ±10%

		VP16RP8M-25			VP16RP8M				
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Units	Conditions
tPD	Input to Output Delay		15	25		20	35	ns	VP16RP8M R1 = 560 Ω R2 = 1.1 KΩ CL = 50 pF VP16RP8M-25 R1 = 200 Ω R2 = 390 Ω CL = 50 pF
tCLK	Clock to Output or Feedback		10	15		15	25	ns	
fMAX	Maximum Frequency	28.5			16			MHz	
tW	Clock Width, LOW	15			25			ns	
	Clock Width, HIGH	15			25			ns	
tSU	Setup Time	25			35			ns	
tH	Hold Time				0			ns	
tPZX	Pin 11 to Output ENABLED		10	20		15	25	ns	R1 = 560 Ω R2 = 240 Ω CL = 5 pF Note 3
tPXZ	Pin 11 to Output DISABLED		10	20		15	25	ns	
tPZI	Input to Output ENABLED		15	25		25	35	ns	
tPIZ	Input to Output DISABLED		15	25		25	35	ns	

Note:
1. All product terms used
2. Only one output is shorted at any one time
3. Sample tested. Timing reference voltages are 100 mV above or below tri-state level set by the resistor divider of the test load.

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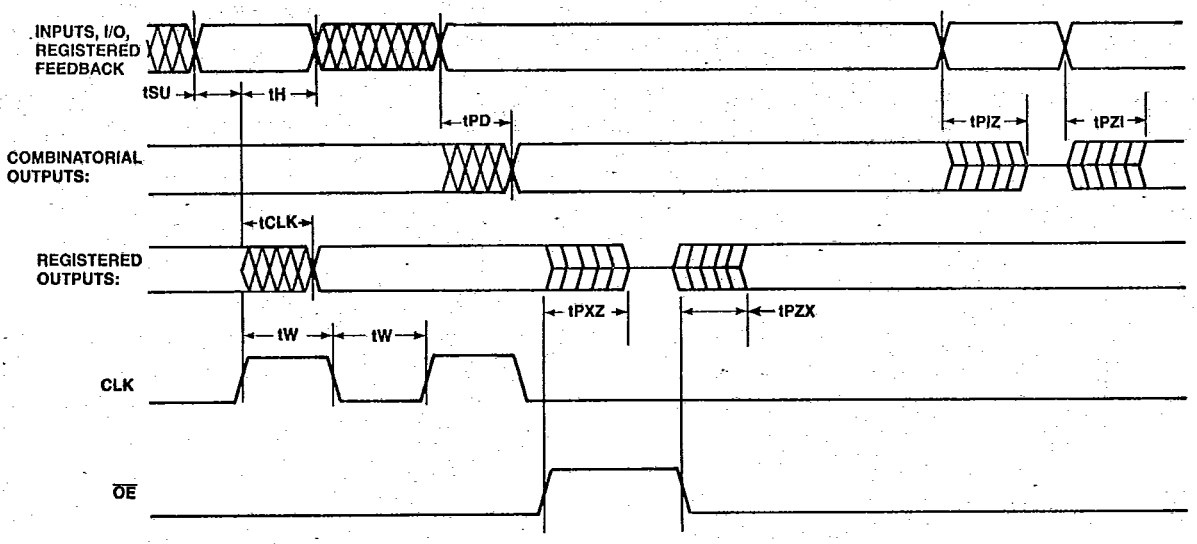
TIMING DIAGRAM



AC TEST CONDITIONS

Input pulse level	0 to 3.0 V
Input rise and fall time, Note 1	6 ns
Innput timing level	1.5 V
Output timing level	1.5 V
Output load	See Figure 1

FIGURE 1.

AC TEST LOAD

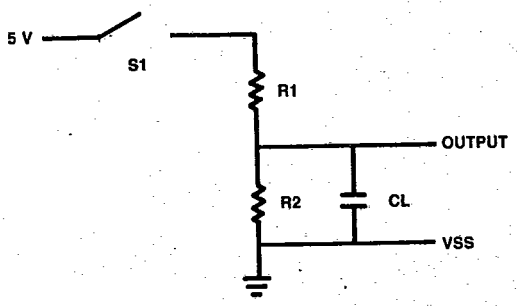
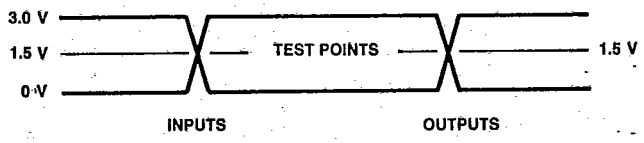


FIGURE 2.

AC TESTING INPUT, OUTPUT WAVEFORM



FOR AC TESTING, HIGH INPUTS ARE DRIVEN AT 3.0 V FOR A LOGIC "1" AND LOW INPUTS ARE DRIVEN AT 0 V FOR A LOGIC "0". TIMING MEASUREMENTS ARE REFERENCED TO 1.5 V AT THE INPUTS AND OUTPUTS.

Notes:

1. Measured at 10% and 90% points of the waveform

PRE-LOAD REQUIREMENTS FOR REGISTERED OUTPUT

The VP16RP8M has circuitry incorporated into the registered outputs to allow these devices to be PRE-LOADed to any desired active HIGH or LOW level. This feature is designed to aid in testing registered devices by forcing defined states into the register to minimize the test time. Test time is reduced since it is no longer necessary to incrementally sequence the inputs to get to a desired state. The pin levels necessary to perform the PRE-LOAD operation are shown in Table 2.

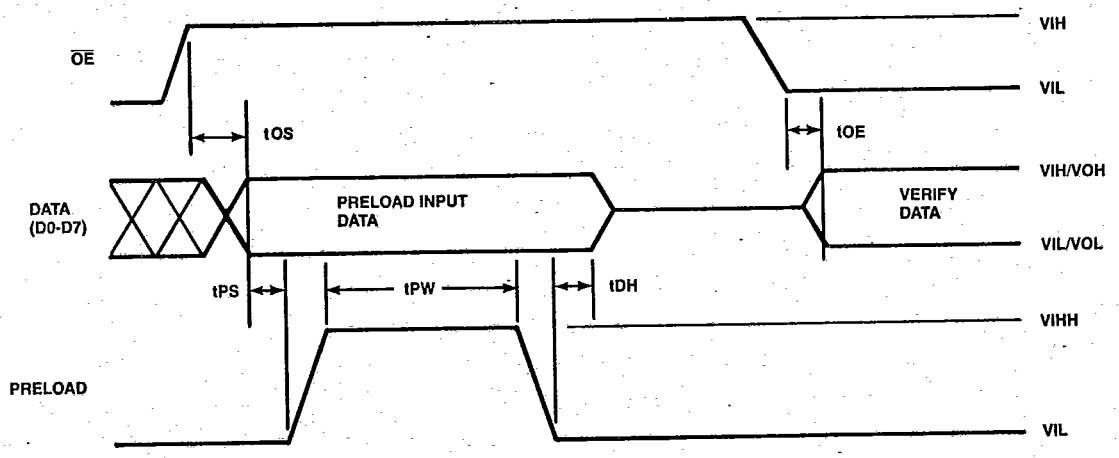
TABLE 2: PIN LEVELS REQUIRED FOR PRE-LOAD

Mode	Pin Numbers										
	1	2	3	4	5	6	7	8	9	11	12–19
PRE-LOAD	X Note 1	X	X	VIHH Note 2	X	X	X	X	X	VIH Note 3	PRE-LOAD INPUTS Note 4
READ PRE-LOAD	Same as Regular Read Operation										

Notes:
1. X = Don't Care TTL Level.
2. VIHH = 9 V, ± 0.5 V.
3. VIH = TTL Input HIGH Level, 2.0 V minimum.
4. Inputs = TTL Input HIGH or LOW Level: Input HIGH = 2.0 V minimum; Input LOW = 0.8 V maximum.

TIMING DIAGRAM

PRE-LOAD



Symbol	Parameter	Min	Max	Units
tOS	Output Enable Setup Time	2		µs
tPS	PRE-LOAD Setup Time	2		µs
tDH	Data Hold Time	2		µs
tPW	PRE-LOAD Pulse Width	2		µs
tOE	Data Valid from /OE		2	µs

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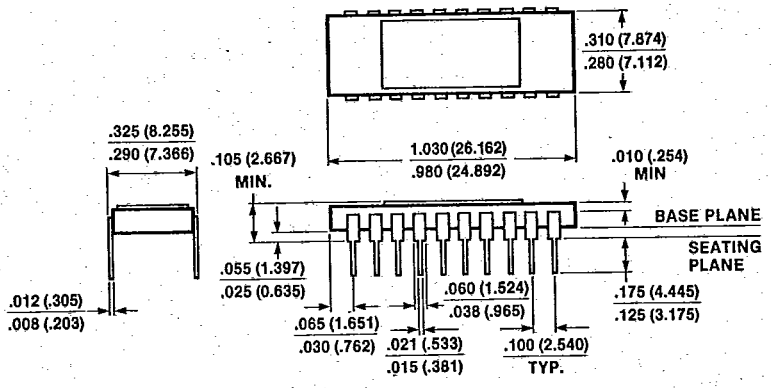
LOGIC DESIGN SUBMISSION MEDIUM

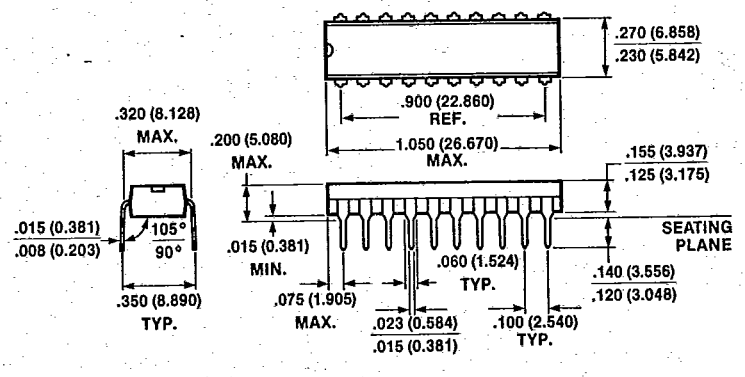
VTI's VP16RP8M is a semicustom logic array that is programmed with the customer's logic equations through the use of a metal mask. Because each set of logic equations requires a new mask, VTI tools a metal mask specifically for each set of equations. In order to insure the correctness of logic equations and mask generation VTI will accept two identically programmed PALs or GALs as the logic equation input. These devices are logically compared on receipt to insure code integrity. VTI reads the devices, automatically enters the logic equations into the design automation system and then outputs a fuse map from the system. Alternatively, VTI will accept Boolean equations or JEDEC files as input. This fuse map will be returned to the customer for verification and sign off before mask and prototype production begin.

PACKAGE OUTLINES

20-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE



20-PIN PLASTIC DUAL IN-LINE



ORDER INFORMATION

VTI assigns a unique, 4-digit code for each logic configuration that is received for processing. This code is referred to as the Programmable Logic code (PL code). After fuse map verification, the 4-digit code becomes part of the VP16RP8M part number and all subsequent order placements must reference this code. Order information is as follows:

Part Number	Access Time	Package
VP16RP8M-25 PC PLXXXX	25 ns	Commercial 0 to 70°C
VP16RP8M-25 CC PLXXXX	25 ns	Commercial 0 to 70°C
VP16RP8M PC PLXXXX	35 ns	Commercial 0 to 70°C
VP16RP8M CC PLXXXX	35 ns	Commercial 0 to 70°C

Notes:
PC suffix = plastic package.
CC suffix = ceramic side-brazed package

VP16RP8M PRELIMINARY

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